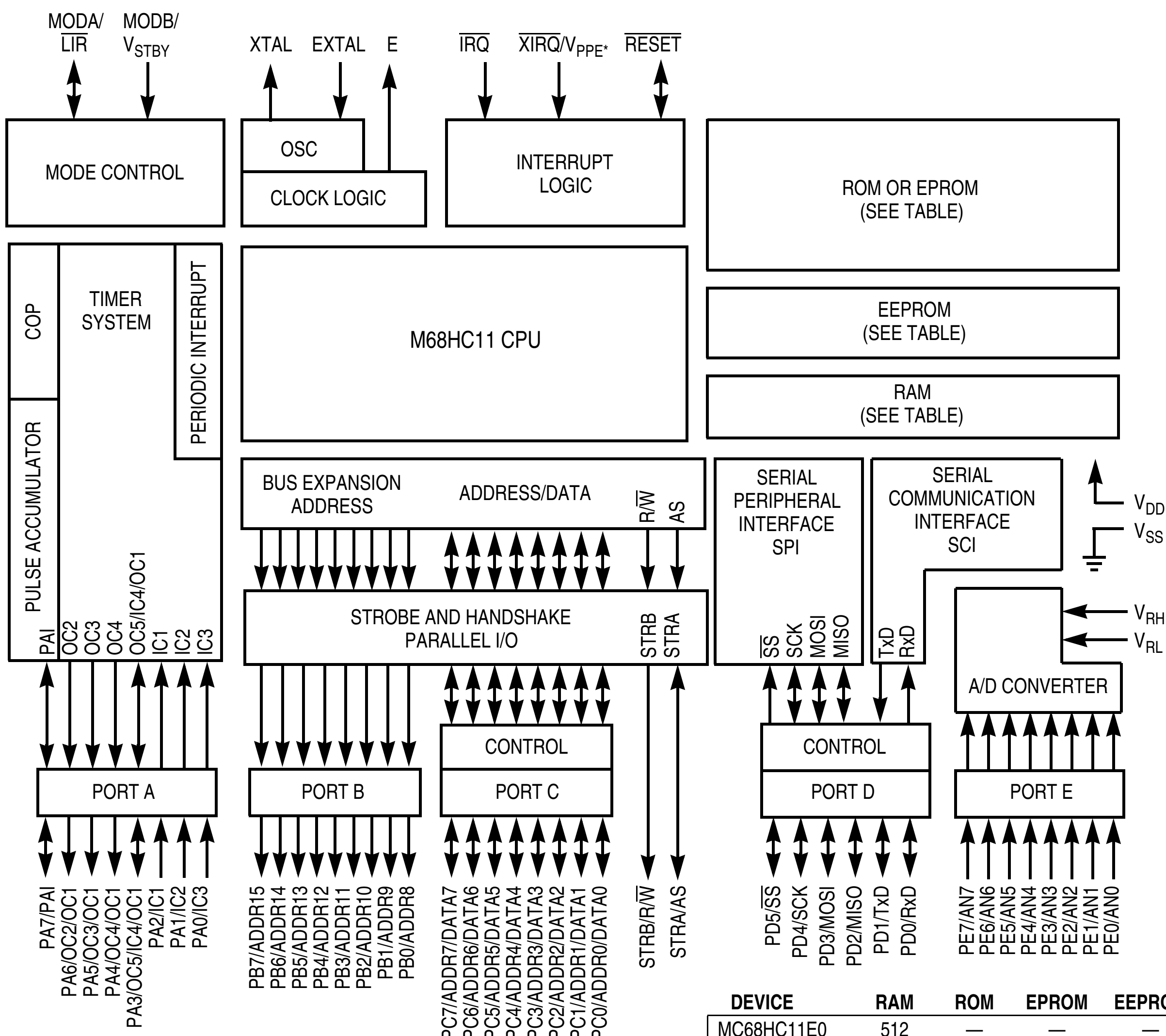
Freescale Semiconductor
Reference Guide

M68HC11ERG
Rev. 2.1, 07/2005

M68HC11E Series Programming Reference Guide

Block Diagram



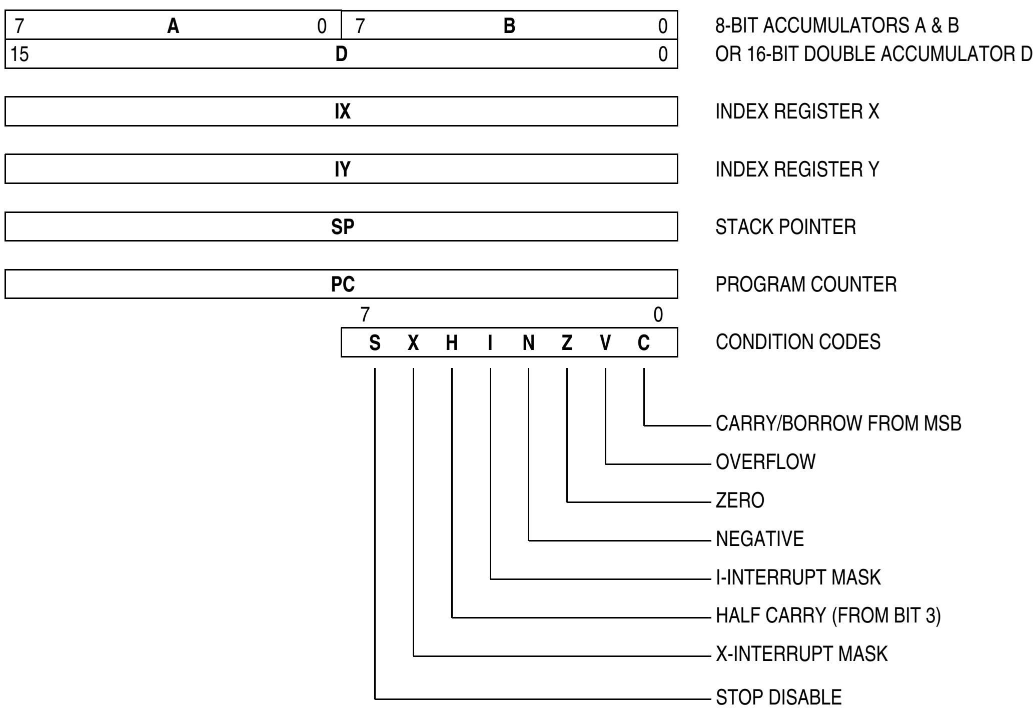
DEVICE	RAM	ROM	EPROM	EEPROM
MC68HC11E0	512	—	—	—
MC68HC11E1	512	—	—	512
MC68HC11E9	512	12 K	—	512
MC68HC711E9	512	—	12 K	512
MC68HC11E20	768	20 K	—	512
MC68HC711E20	768	—	20 K	512
MC68HC811E2	256	—	—	2048

* V_{PPE} applies only to devices with EPROM/OTPROM.

Devices Covered in This Reference Guide

Device	RAM	ROM	EPROM	EEPROM
MC68HC11E0	512	—	—	—
MC68HC11E1	512	—	—	512
MC68HC11E9	512	12K	—	512
MC68HC711E9	512	—	12K	512
MC68HC11E20	768	20K	—	512
MC68HC711E20	768	—	10K	512
MC68HC811E2	256	—	—	2048

M68HC11E Series Programming Model



Crystal Dependent Timer Summary

	Selected Crystal	Common XTAL Frequencies		
		4.0 MHz	**8.0 MHz**	**12.0 MHz**
CPU Clock	**(E)**	**1.0 MHz**	**2.0 MHz**	**3.0 MHz**
Cycle Time	**(1/E)**	**1000 ns**	**500 ns**	**333 ns**
	Pulse Accumulator (in Gated Mode)			
($E/2^6$) ($E/2^{14}$)	1 count — overflow —	64.0 µs 16.384 ms	32.0 µs 8.192 ms	21.330 µs 5.491 ms
	PR[1:0]	Main Timer Count Rates		
($E/1$) ($E/2^{16}$)	0 0 1 count — overflow —	1.0 µs 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms
($E/4$) ($E/2^{18}$)	0 1 1 count — overflow —	4.0 µs 262.14 ms	2.0 µs 131.07 ms	1.333 µs 87.381 ms
($E/8$) ($E/2^{19}$)	1 0 1 count — overflow —	8.0 µs 524.29 ms	4.0 µs 262.14 ms	2.667 µs 174.76 ms
($E/16$) ($E/2^{20}$)	1 1 1 count — overflow —	16.0 µs 1.049 s	8.0 µs 524.29 ms	5.333 µs 349.52 ms
	RTR[1:0]	Periodic (RTI) Interrupt Rates		
($E/2^{13}$) ($E/2^{14}$) ($E/2^{15}$) ($E/2^{16}$)	0 0 0 1 1 0 1 1	8.192 ms 16.384 ms 32.768 ms 65.536 ms	4.096 ms 8.192 ms 16.384 ms 32.768 ms	2.731 ms 5.461 ms 10.923 ms 21.845 ms
	CR[1:0]	COP Watchdog Timeout Rates		
($E/2^{15}$) ($E/2^{17}$) ($E/2^{19}$) ($E/2^{21}$)	0 0 0 1 1 0 1 1	32.768 ms 131.072 ms 524.288 ms 2.097 s	16.384 ms 65.536 ms 262.14 ms 1.049 s	10.923 ms 43.691 ms 174.76 ms 699.05 ms
($E/2^{15}$)	Timeout tolerance (–0 ms/+...)	32.8 ms	16.4 ms	10.9 ms

Interrupt Vector Assignments

Vector Address	Interrupt Source	CCR Mask Bit	Local Mask
FFC0, C1 – FFD4, D5	Reserved	—	—
FFD6, D7	SCI serial system[1] • SCI receive data register full • SCI receiver overrun • SCI transmit data register empty • SCI transmit complete • SCI idle line detect	I	 RIE RIE TIE TCIE ILIE
FFD8, D9	SPI serial transfer complete	I	SPIE
FFDA, DB	Pulse accumulator input edge	I	PAII
FFDC, DD	Pulse accumulator overflow	I	PAOVI
FFDE, DF	Timer overflow	I	TOI
FFE0, E1	Timer input capture 4/output compare 5	I	I4/O5I
FFE2, E3	Timer output compare 4	I	OC4I
FFE4, E5	Timer output compare 3	I	OC3I
FFE6, E7	Timer output compare 2	I	OC2I
FFE8, E9	Timer output compare 1	I	OC1I
FFEA, EB	Timer input capture 3	I	IC3I
FFEC, ED	Timer input capture 2	I	IC2I
FFEE, EF	Timer input capture 1	I	IC1I
FFF0, F1	Real-time interrupt	I	RTII
FFF2, F3	$\overline{\text{IRQ}}$ (external pin)	I	None
FFF4, F5	$\overline{\text{XIRQ}}$ pin	X	None
FFF6, F7	Software interrupt	None	None
FFF8, F9	Illegal opcode trap	None	None
FFFA, FB	COP failure	None	NOCOP
FFFC, FD	Clock monitor fail	None	CME
FFFE, FF	$\overline{\text{RESET}}$	None	None

NOTES:
1. Interrupts generated by SCI; read SCSR to determine source. Refer to HPRIO register to determine priority of interrupt.

M68HC11E Series Memory Maps

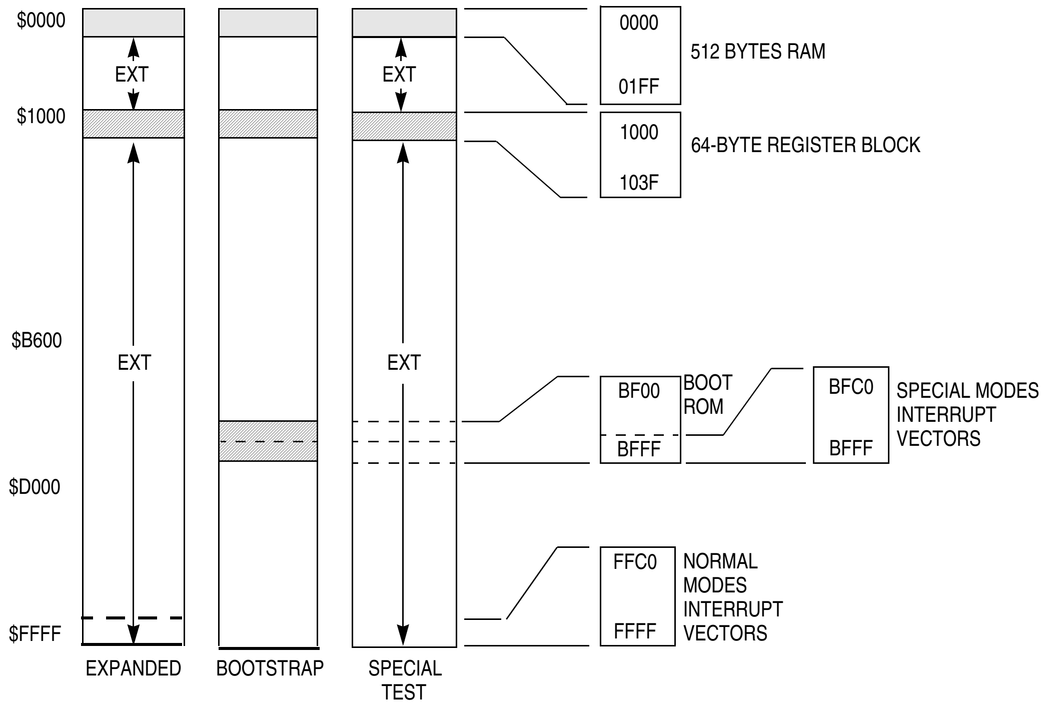


Figure 1. Memory Map for MC68HC11E0

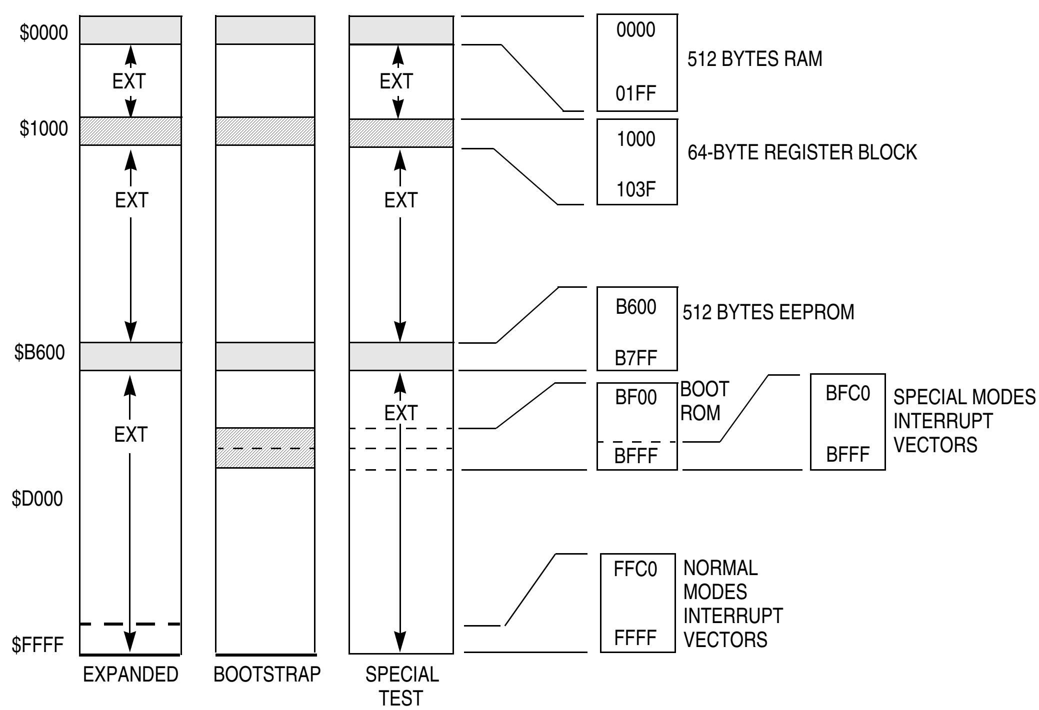


Figure 2. Memory Map for MC68HC11E1

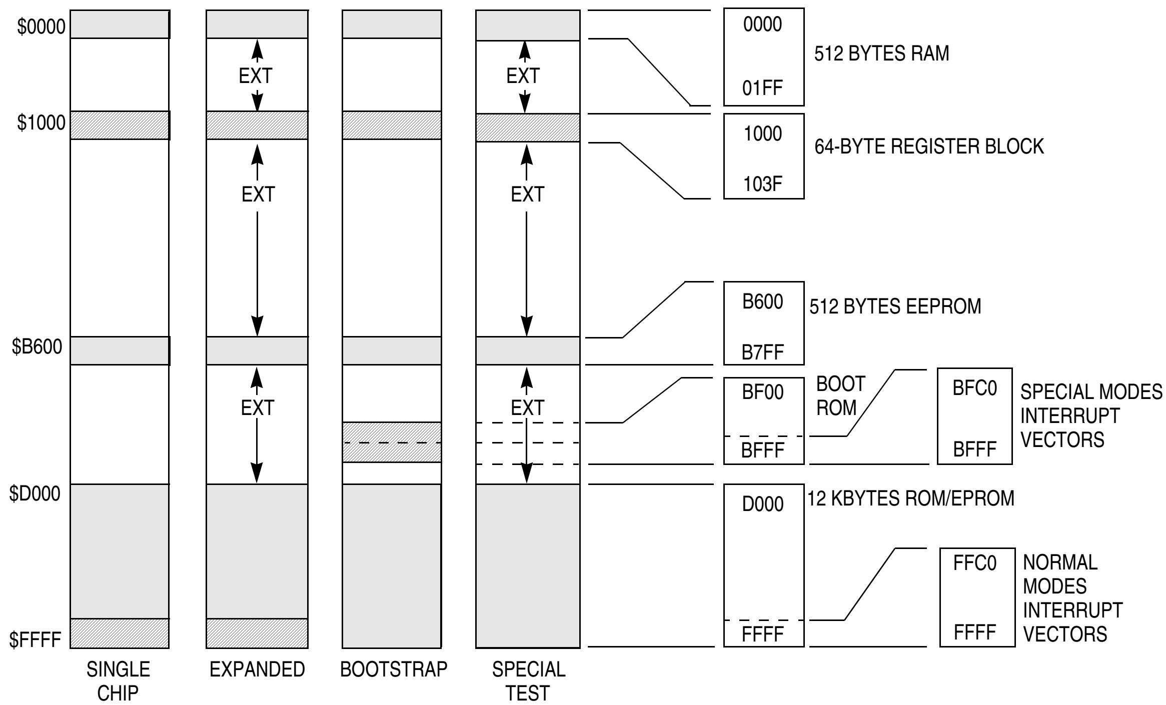
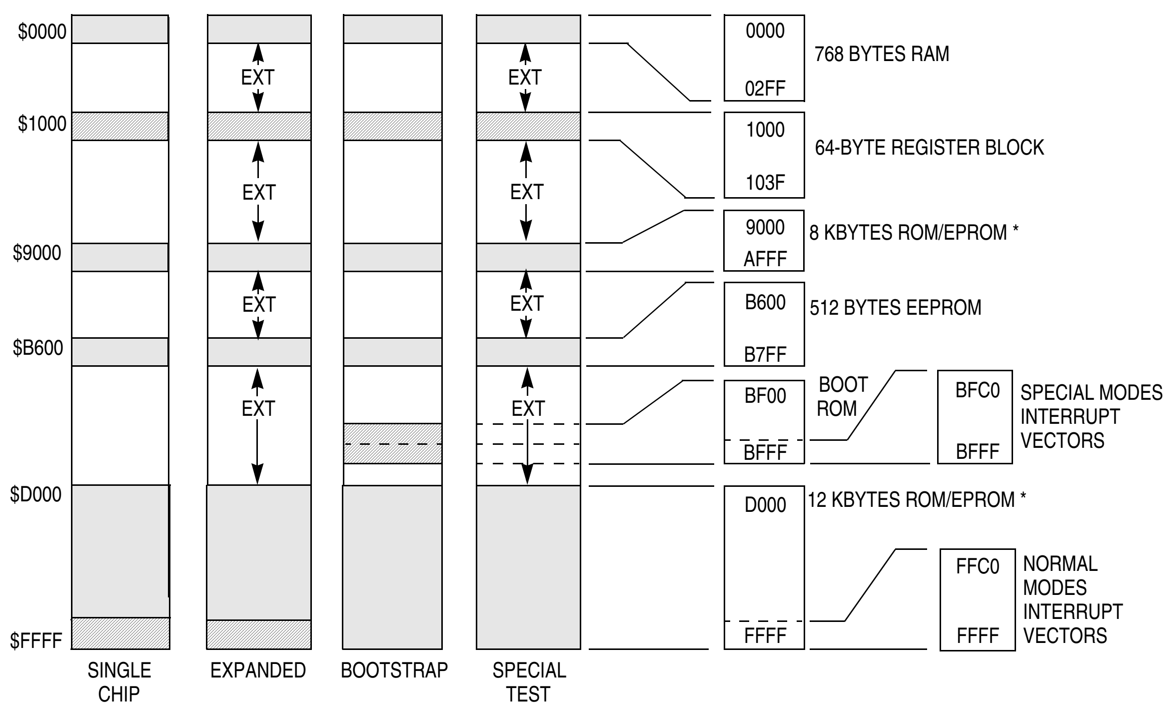


Figure 3. Memory Map for MC68HC(7)11E9



* 20 Kbytes ROM/EPROM are contained in two segments of 8 Kbytes and 12 Kbytes each.

Figure 4. Memory Map for MC68HC(7)11E20

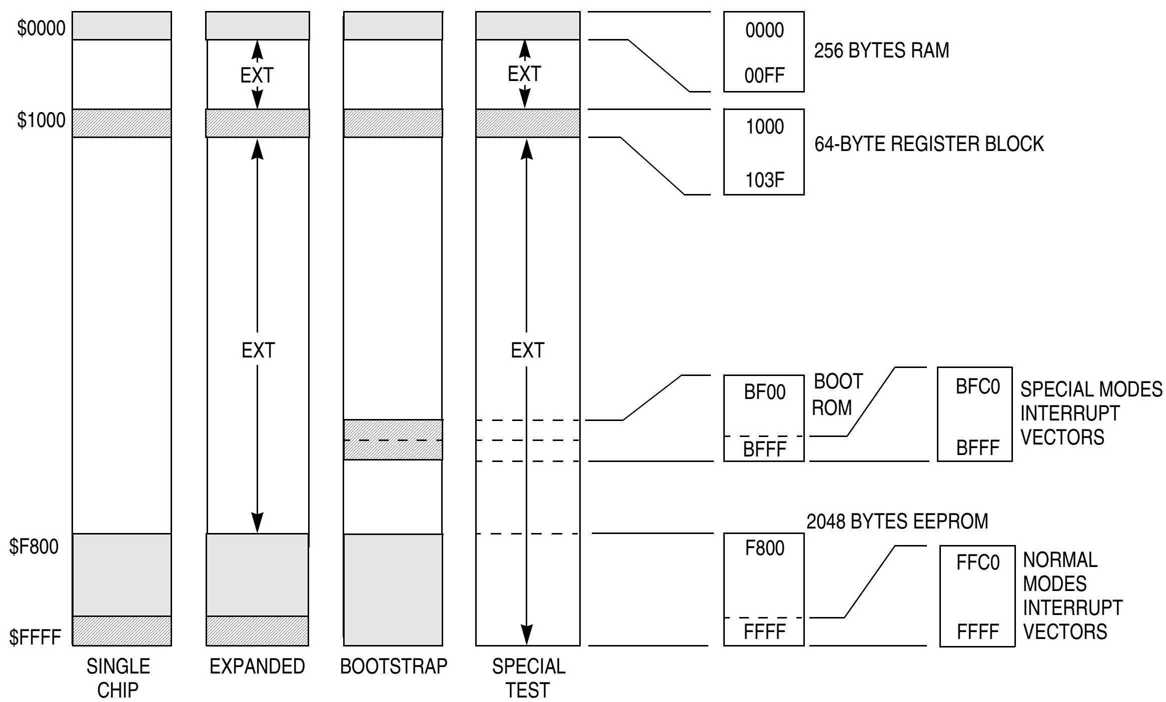


Figure 5. Memory Map for MC68HC811E2

Opcode Maps

The opcode maps are shown on the following pages.

Page 1

DIR

LSB \ MSB										ACCA				ACCB				
		INH	INH	REL	INH	ACCA	ACCB	IND,X	EXT	IMM	DIR	IND,X	EXT	IMM	DIR	IND,X	EXT	
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0	TEST	SBA	BRA	TSX	NEG				SUB								0
0001	1	NOP	CBA	BRN	INS					CMP								1
0010	2	IDIV	BRSET	BHI	PULA					SBC								2
0011	3	EDIV	BRCLR	BLS	PULB	COM				SUBD				ADDD				3
0100	4	LSRD	BSET	BCC	DES	LSR				AND								4
0101	5	ASLD	BCLR	BCS	TXS					BIT								5
0110	6	TAP	TAB	BNE	PSHA	ROR				LDA								6
0111	7	TPA	TBA	BEQ	PSHB	ASR					STA				STA			7
1000	8	INX	PAGE 2	BVC	PULX	ASL				EOR								8
1001	9	DEX	DAA	BVS	RTS	ROL				ADC								9
1010	A	CLV	PAGE 3	BPL	ABX	DEC				ORA								A
1011	B	SEV	ABA	BMI	RTI					ADD								B
1100	C	CLC	BSET	BGE	PSHX	INC				CPX				LDD				C
1101	D	SEC	BCLR	BLT	MUL	TST				BSR	JSR			PAGE 4	STD			D
1110	E	CLI	BRSET	BGT	WAI			JMP		LDS				LDX				E
1111	F	SEI	BRCLR	BLE	SWI	CLR				XGDX	STS			STOP	STX			F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

IND,X

Page 2 (18XX)

										ACCA				ACCB				
		INH			INH			IND,Y		IMM	DIR	IND,X	EXT	IMM	DIR	IND,X	EXT	
LSB \ MSB		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0				TSY			NEG				SUB				SUB		0
0001	1											CMP				CMP		1
0010	2											SBC				SBC		2
0011	3							COM				SUBD				ADDD		3
0100	4							LSR				AND				AND		4
0101	5				TYS							BIT				BIT		5
0110	6							ROR				LDA				LDA		6
0111	7							ASR				STA				STA		7
1000	8	INY			PULY			ASL				EOR				EOR		8
1001	9	DEY						RDL				ADC				ADC		9
1010	A				ABY			DEC				ORA				ORA		A
1011	B											ADD				ADD		B
1100	C		BSET		PSHY			INC		CPY						LDD		C
1101	D		BCLR					TST				JSR				STD		D
1110	E		BRSET					JMP				LDS		LDY				E
1111	F		BRCLR					CLR		XGDY		STS			STY			F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

IND,Y

Page 3 (1AXX)

										ACCA				ACCB				
										IMM	DIR	IND,X	EXT			IND,X		
LSB \ MSB		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0																	0
0001	1																	1
0010	2																	2
0011	3									CPD								3
0100	4																	4
0101	5																	5
0110	6																	6
0111	7																	7
1000	8																	8
1001	9																	9
1010	A																	A
1011	B																	B
1100	C											CPY						C
1101	D																	D
1110	E															LDY		E
1111	F															STY		F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Page 4 (CDXX)

										ACCA				ACCB				
												IND,Y				IND,Y		
LSB \ MSB		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0																	0
0001	1																	1
0010	2																	2
0011	3											CPD						3
0100	4																	4
0101	5																	5
0110	6																	6
0111	7																	7
1000	8																	8
1001	9																	9
1010	A																	A
1011	B																	B
1100	C											CPX						C
1101	D																	D
1110	E															LDX		E
1111	F															STX		F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Branches

Simple Branches

Mnemonic	Opcode	Cycles
BRA	20	3
BRN	21	3
BSR	8D	7

Simple Conditional Branches

Test	True		False	
	Instruction	Opcode	Instruction	Opcode
N = 1	BMI	2B	BPL	2A
Z = 1	BEQ	27	BNE	26
V = 1	BVS	29	BVC	28
C = 1	BCS	25	BCC	24

Signed Conditional Branches

Test	True		False	
	Instruction	Opcode	Instruction	Opcode
r > m	BGT	2E	BLE	2F
r ≥ m	BGE	2C	BLT	2D
r = m	BEQ	27	BNE	26
r ≤ m	BLE	2F	BGT	2E
r < m	BLT	2D	BGE	2C

Unsigned Conditional Branches

Test	True		False	
	Instruction	Opcode	Instruction	Opcode
r > m	BHI	22	BLS	23
r ≥ m	BHS/BCC	24	BL0/BCS	25
r = m	BEQ	27	BNE	26
r ≤ m	BLS	23	BHI	22
r < m	BLO/BCS	25	BHS/BCC	24

Bit Manipulation Branches

BRCLR

Branch if all selected bits are clear (opcode) (operand addr) (mask) (rel offset)
M • mm = 0? M = operand in memory; mm = mask

BRSET

Branch if all selected bits are set (opcode) (operand addr) (rel offset)
($\overline{M}$) • mm = 0? M = operand in memory; mm = mask

Instruction Set

Refer to Table 1, which shows all the M68HC11 instructions in all possible addressing modes. For each instruction, the table shows the operand construction, the number of machine code bytes, and execution time in CPU E-clock cycles.

Table 1. Instruction Set (Sheet 1 of 8)

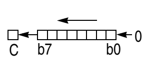
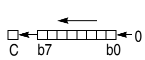
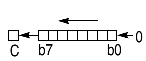
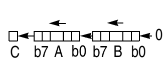
Mnemonic	Operation	Description	Addressing Mode	Instruction Opcode	Instruction Operand	Instruction Cycles	S	X	H	I	N	Z	V	C
ABA	Add Accumulators	A + B ⇒ A	INH	1B	—	2	—	—	Δ	—	Δ	Δ	Δ	Δ
ABX	Add B to X	IX + (00 : B) ⇒ IX	INH	3A	—	3	—	—	—	—	—	—	—	—
ABY	Add B to Y	IY + (00 : B) ⇒ IY	INH	18 3A	—	4	—	—	—	—	—	—	—	—
ADCA (opr)	Add with Carry to A	A + M + C ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	89 99 B9 A9 18 A9	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADCB (opr)	Add with Carry to B	B + M + C ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C9 D9 F9 E9 18 E9	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADDA (opr)	Add Memory to A	A + M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	8B 9B BB AB 18 AB	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADDB (opr)	Add Memory to B	B + M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	CB DB FB EB 18 EB	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADDD (opr)	Add 16-Bit to D	D + (M : M + 1) ⇒ D	IMM DIR EXT IND,X IND,Y	C3 D3 F3 E3 18 E3	jj kk dd hh ll ff ff	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ANDA (opr)	AND A with Memory	A • M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	84 94 B4 A4 18 A4	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
ANDB (opr)	AND B with Memory	B • M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C4 D4 F4 E4 18 E4	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
ASL (opr)	Arithmetic Shift Left		EXT IND,X IND,Y	78 68 18 68	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ASLA	Arithmetic Shift Left A		A INH	48	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASLB	Arithmetic Shift Left B		B INH	58	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASLD	Arithmetic Shift Left D		INH	05	—	3	—	—	—	—	Δ	Δ	Δ	Δ

Table 1. Instruction Set (Sheet 2 of 8)

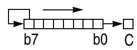
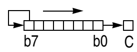
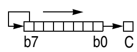
Mnemonic	Operation	Description	Addressing Mode	Instruction Opcode	Instruction Operand	Instruction Cycles	S	X	H	I	N	Z	V	C
ASR	Arithmetic Shift Right		EXT IND,X IND,Y	77 67 18 67	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ASRA	Arithmetic Shift Right A		A INH	47	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASRB	Arithmetic Shift Right B		B INH	57	—	2	—	—	—	—	Δ	Δ	Δ	Δ
BCC (rel)	Branch if Carry Clear	? C = 0	REL	24	rr	3	—	—	—	—	—	—	—	—
BCLR (opr) (msk)	Clear Bit(s)	M • ($\overline{mm}$) ⇒ M	DIR IND,X IND,Y	15 1D 18 1D	dd mm ff mm ff mm	6 7 8	—	—	—	—	Δ	Δ	0	—
BCS (rel)	Branch if Carry Set	? C = 1	REL	25	rr	3	—	—	—	—	—	—	—	—
BEQ (rel)	Branch if = Zero	? Z = 1	REL	27	rr	3	—	—	—	—	—	—	—	—
BGE (rel)	Branch if Δ Zero	? N ⊕ V = 0	REL	2C	rr	3	—	—	—	—	—	—	—	—
BGT (rel)	Branch if > Zero	? Z + (N ⊕ V) = 0	REL	2E	rr	3	—	—	—	—	—	—	—	—
BHI (rel)	Branch if Higher	? C + Z = 0	REL	22	rr	3	—	—	—	—	—	—	—	—
BHS (rel)	Branch if Higher or Same	? C = 0	REL	24	rr	3	—	—	—	—	—	—	—	—
BITA (opr)	Bit(s) Test A with Memory	A • M	A IMM A DIR A EXT A IND,X A IND,Y	85 95 B5 A5 18 A5	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
BITB (opr)	Bit(s) Test B with Memory	B • M	B IMM B DIR B EXT B IND,X B IND,Y	C5 D5 F5 E5 18 E5	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
BLE (rel)	Branch if Δ Zero	? Z + (N ⊕ V) = 1	REL	2F	rr	3	—	—	—	—	—	—	—	—
BLO (rel)	Branch if Lower	? C = 1	REL	25	rr	3	—	—	—	—	—	—	—	—
BLS (rel)	Branch if Lower or Same	? C + Z = 1	REL	23	rr	3	—	—	—	—	—	—	—	—
BLT (rel)	Branch if < Zero	? N ⊕ V = 1	REL	2D	rr	3	—	—	—	—	—	—	—	—
BMI (rel)	Branch if Minus	? N = 1	REL	2B	rr	3	—	—	—	—	—	—	—	—
BNE (rel)	Branch if not = Zero	? Z = 0	REL	26	rr	3	—	—	—	—	—	—	—	—
BPL (rel)	Branch if Plus	? N = 0	REL	2A	rr	3	—	—	—	—	—	—	—	—
BRA (rel)	Branch Always	? 1 = 1	REL	20	rr	3	—	—	—	—	—	—	—	—
BRCLR(opr) (msk) (rel)	Branch if Bit(s) Clear	? M • mm = 0	DIR IND,X IND,Y	13 1F 18 1F	dd mm rr ff mm rr ff mm rr	6 7 8	—	—	—	—	—	—	—	—
BRN (rel)	Branch Never	? 1 = 0	REL	21	rr	3	—	—	—	—	—	—	—	—
BRSET(opr) (msk) (rel)	Branch if Bit(s) Set	? ($\overline{M}$) • mm = 0	DIR IND,X IND,Y	12 1E 18 1E	dd mm rr ff mm rr ff mm rr	6 7 8	—	—	—	—	—	—	—	—
BSET (opr) (msk)	Set Bit(s)	M + mm ⇒ M	DIR IND,X IND,Y	14 1C 18 1C	dd mm ff mm ff mm	6 7 8	—	—	—	—	Δ	Δ	0	—
BSR (rel)	Branch to Subroutine	See Figure 3–2	REL	8D	rr	6	—	—	—	—	—	—	—	—
BVC (rel)	Branch if Overflow Clear	? V = 0	REL	28	rr	3	—	—	—	—	—	—	—	—

Table 1. Instruction Set (Sheet 3 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
BVS (rel)	Branch if Overflow Set	? V = 1	REL	29	rr	3	—	—	—	—	—	—	—	—
CBA	Compare A to B	A – B	INH	11	—	2	—	—	—	—	Δ	Δ	Δ	Δ
CLC	Clear Carry Bit	0 ⇒ C	INH	0C	—	2	—	—	—	—	—	—	—	0
CLI	Clear Interrupt Mask	0 ⇒ I	INH	0E	—	2	—	—	—	0	—	—	—	—
CLR (opr)	Clear Memory Byte	0 ⇒ M	EXT IND,X IND,Y	7F 6F 18 6F	hh ll ff ff	6 6 7	—	—	—	—	0	1	0	0
CLRA	Clear Accumulator A	0 ⇒ A	A INH	4F	—	2	—	—	—	—	0	1	0	0
CLRB	Clear Accumulator B	0 ⇒ B	B INH	5F	—	2	—	—	—	—	0	1	0	0
CLV	Clear Overflow Flag	0 ⇒ V	INH	0A	—	2	—	—	—	—	—	—	0	—
CMPA (opr)	Compare A to Memory	A – M	A IMM A DIR A EXT A IND,X A IND,Y	81 91 B1 A1 18 A1	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
CMPB (opr)	Compare B to Memory	B – M	B IMM B DIR B EXT B IND,X B IND,Y	C1 D1 F1 E1 18 E1	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
COM (opr)	Ones Complement Memory Byte	$FF – M ⇒ M	EXT IND,X IND,Y	73 63 18 63	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	0	1
COMA	Ones Complement A	$FF – A ⇒ A	A INH	43	—	2	—	—	—	—	Δ	Δ	0	1
COMB	Ones Complement B	$FF – B ⇒ B	B INH	53	—	2	—	—	—	—	Δ	Δ	0	1
CPD (opr)	Compare D to Memory 16-Bit	D – M : M + 1	IMM DIR EXT IND,X IND,Y	1A 83 1A 93 1A B3 1A A3 CD A3	jj kk dd hh ll ff ff	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
CPX (opr)	Compare X to Memory 16-Bit	IX – M : M + 1	IMM DIR EXT IND,X IND,Y	8C 9C BC AC CD AC	jj kk dd hh ll ff ff	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
CPY (opr)	Compare Y to Memory 16-Bit	IY – M : M + 1	IMM DIR EXT IND,X IND,Y	18 8C 18 9C 18 BC 1A AC 18 AC	jj kk dd hh ll ff ff	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
DAA	Decimal Adjust A	Adjust Sum to BCD	INH	19	—	2	—	—	—	—	Δ	Δ	Δ	Δ
DEC (opr)	Decrement Memory Byte	M – 1 ⇒ M	EXT IND,X IND,Y	7A 6A 18 6A	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	—
DECA	Decrement Accumulator A	A – 1 ⇒ A	A INH	4A	—	2	—	—	—	—	Δ	Δ	Δ	—
DECB	Decrement Accumulator B	B – 1 ⇒ B	B INH	5A	—	2	—	—	—	—	Δ	Δ	Δ	—

Table 1. Instruction Set (Sheet 4 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
DES	Decrement Stack Pointer	SP – 1 ⇒ SP	INH	34	—	3	—	—	—	—	—	—	—	—
DEX	Decrement Index Register X	IX – 1 ⇒ IX	INH	09	—	3	—	—	—	—	—	Δ	—	—
DEY	Decrement Index Register Y	IY – 1 ⇒ IY	INH	18 09	—	4	—	—	—	—	—	Δ	—	—
EORA (opr)	Exclusive OR A with Memory	A ⊕ M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	88 98 B8 A8 18 A8	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
EORB (opr)	Exclusive OR B with Memory	B ⊕ M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C8 D8 F8 E8 18 E8	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
FDIV	Fractional Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	03	—	41	—	—	—	—	—	Δ	Δ	Δ
IDIV	Integer Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	02	—	41	—	—	—	—	—	Δ	0	Δ
INC (opr)	Increment Memory Byte	M + 1 ⇒ M	EXT IND,X IND,Y	7C 6C 18 6C	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	—
INCA	Increment Accumulator A	A + 1 ⇒ A	A INH	4C	—	2	—	—	—	—	Δ	Δ	Δ	—
INCB	Increment Accumulator B	B + 1 ⇒ B	B INH	5C	—	2	—	—	—	—	Δ	Δ	Δ	—
INS	Increment Stack Pointer	SP + 1 ⇒ SP	INH	31	—	3	—	—	—	—	—	—	—	—
INX	Increment Index Register X	IX + 1 ⇒ IX	INH	08	—	3	—	—	—	—	—	Δ	—	—
INY	Increment Index Register Y	IY + 1 ⇒ IY	INH	18 08	—	4	—	—	—	—	—	Δ	—	—
JMP (opr)	Jump	See Figure 3–2	EXT IND,X IND,Y	7E 6E 18 6E	hh ll ff ff	3 3 4	—	—	—	—	—	—	—	—
JSR (opr)	Jump to Subroutine	See Figure 3–2	DIR EXT IND,X IND,Y	9D BD AD 18 AD	dd hh ll ff ff	5 6 6 7	—	—	—	—	—	—	—	—
LDAA (opr)	Load Accumulator A	M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	86 96 B6 A6 18 A6	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
LDAB (opr)	Load Accumulator B	M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C6 D6 F6 E6 18 E6	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
LDD (opr)	Load Double Accumulator D	M ⇒ A,M + 1 ⇒ B	IMM DIR EXT IND,X IND,Y	CC DC FC EC 18 EC	jj kk dd hh ll ff ff	3 4 5 5 6	—	—	—	—	Δ	Δ	0	—

Table 1. Instruction Set (Sheet 5 of 8)

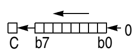
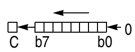
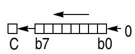
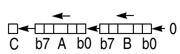
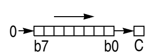
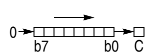
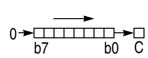
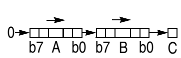
Mnemonic	Operation	Description	Addressing Mode	Instruction Opcode	Instruction Operand	Instruction Cycles	S	X	H	I	N	Z	V	C
LDS (opr)	Load Stack Pointer	M : M + 1 ⇒ SP	IMM DIR EXT IND,X IND,Y	8E 9E BE AE 18 AE	jj kk dd hh ll ff ff	3 4 5 5 6	—	—	—	—	Δ	Δ	0	—
LDX (opr)	Load Index Register X	M : M + 1 ⇒ IX	IMM DIR EXT IND,X IND,Y	CE DE FE EE CD EE	jj kk dd hh ll ff ff	3 4 5 5 6	—	—	—	—	Δ	Δ	0	—
LDY (opr)	Load Index Register Y	M : M + 1 ⇒ IY	IMM DIR EXT IND,X IND,Y	18 CE 18 DE 18 FE 1A EE 18 EE	jj kk dd hh ll ff ff	4 5 6 6 6	—	—	—	—	Δ	Δ	0	—
LSL (opr)	Logical Shift Left		EXT IND,X IND,Y	78 68 18 68	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
LSLA	Logical Shift Left A		A INH	48	—	2	—	—	—	—	Δ	Δ	Δ	Δ
LSLB	Logical Shift Left B		B INH	58	—	2	—	—	—	—	Δ	Δ	Δ	Δ
LSLD	Logical Shift Left Double		INH	05	—	3	—	—	—	—	Δ	Δ	Δ	Δ
LSR (opr)	Logical Shift Right		EXT IND,X IND,Y	74 64 18 64	hh ll ff ff	6 6 7	—	—	—	—	0	Δ	Δ	Δ
LSRA	Logical Shift Right A		A INH	44	—	2	—	—	—	—	0	Δ	Δ	Δ
LSRB	Logical Shift Right B		B INH	54	—	2	—	—	—	—	0	Δ	Δ	Δ
LSRD	Logical Shift Right Double		INH	04	—	3	—	—	—	—	0	Δ	Δ	Δ
MUL	Multiply 8 by 8	A ∗ B ⇒ D	INH	3D	—	10	—	—	—	—	—	—	—	Δ
NEG (opr)	Two's Complement Memory Byte	0 – M ⇒ M	EXT IND,X IND,Y	70 60 18 60	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
NEGA	Two's Complement A	0 – A ⇒ A	A INH	40	—	2	—	—	—	—	Δ	Δ	Δ	Δ
NEGB	Two's Complement B	0 – B ⇒ B	B INH	50	—	2	—	—	—	—	Δ	Δ	Δ	Δ
NOP	No operation	No Operation	INH	01	—	2	—	—	—	—	—	—	—	—
ORAA (opr)	OR Accumulator A (Inclusive)	A + M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	8A 9A BA AA 18 AA	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
ORAB (opr)	OR Accumulator B (Inclusive)	B + M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	CA DA FA EA 18 EA	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—

Table 1. Instruction Set (Sheet 6 of 8)

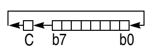
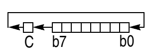
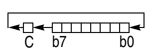
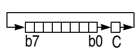
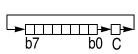
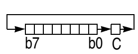
Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
PSHA	Push A onto Stack	A ⇒ Stk,SP = SP – 1	A INH	36	—	3	—	—	—	—	—	—	—	—
PSHB	Push B onto Stack	B ⇒ Stk,SP = SP – 1	B INH	37	—	3	—	—	—	—	—	—	—	—
PSHX	Push X onto Stack (Lo First)	IX ⇒ Stk,SP = SP – 2	INH	3C	—	4	—	—	—	—	—	—	—	—
PSHY	Push Y onto Stack (Lo First)	IY ⇒ Stk,SP = SP – 2	INH	18 3C	—	5	—	—	—	—	—	—	—	—
PULA	Pull A from Stack	SP = SP + 1, A ⇐ Stk	A INH	32	—	4	—	—	—	—	—	—	—	—
PULB	Pull B from Stack	SP = SP + 1, B ⇐ Stk	B INH	33	—	4	—	—	—	—	—	—	—	—
PULX	Pull X From Stack (Hi First)	SP = SP + 2, IX ⇐ Stk	INH	38	—	5	—	—	—	—	—	—	—	—
PULY	Pull Y from Stack (Hi First)	SP = SP + 2, IY ⇐ Stk	INH	18 38	—	6	—	—	—	—	—	—	—	—
ROL (opr)	Rotate Left		EXT IND,X IND,Y	79 69 18 69	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ROLA	Rotate Left A		A INH	49	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ROLB	Rotate Left B		B INH	59	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ROR (opr)	Rotate Right		EXT IND,X IND,Y	76 66 18 66	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
RORA	Rotate Right A		A INH	46	—	2	—	—	—	—	Δ	Δ	Δ	Δ
RORB	Rotate Right B		B INH	56	—	2	—	—	—	—	Δ	Δ	Δ	Δ
RTI	Return from Interrupt	See Figure 3–2	INH	3B	—	12	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
RTS	Return from Subroutine	See Figure 3–2	INH	39	—	5	—	—	—	—	—	—	—	—
SBA	Subtract B from A	A – B ⇒ A	INH	10	—	2	—	—	—	—	Δ	Δ	Δ	Δ
SBCA (opr)	Subtract with Carry from A	A – M – C ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	82 92 B2 A2 18 A2	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
SBCB (opr)	Subtract with Carry from B	B – M – C ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C2 D2 F2 E2 18 E2	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
SEC	Set Carry	1 ⇒ C	INH	0D	—	2	—	—	—	—	—	—	—	1
SEI	Set Interrupt Mask	1 ⇒ I	INH	0F	—	2	—	—	—	1	—	—	—	—
SEV	Set Overflow Flag	1 ⇒ V	INH	0B	—	2	—	—	—	—	—	—	1	—

Table 1. Instruction Set (Sheet 7 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
STAA (opr)	Store Accumulator A	A ⇒ M	A DIR A EXT A IND,X A IND,Y	97 B7 A7 18 A7	dd hh ll ff ff	3 4 4 5	—	—	—	—	Δ	Δ	0	—
STAB (opr)	Store Accumulator B	B ⇒ M	B DIR B EXT B IND,X B IND,Y	D7 F7 E7 18 E7	dd hh ll ff ff	3 4 4 5	—	—	—	—	Δ	Δ	0	—
STD (opr)	Store Accumulator D	A ⇒ M, B ⇒ M + 1	DIR EXT IND,X IND,Y	DD FD ED 18 ED	dd hh ll ff ff	4 5 5 6	—	—	—	—	Δ	Δ	0	—
STOP	Stop Internal Clocks	—	INH	CF	—	2	—	—	—	—	—	—	—	—
STS (opr)	Store Stack Pointer	SP ⇒ M : M + 1	DIR EXT IND,X IND,Y	9F BF AF 18 AF	dd hh ll ff ff	4 5 5 6	—	—	—	—	Δ	Δ	0	—
STX (opr)	Store Index Register X	IX ⇒ M : M + 1	DIR EXT IND,X IND,Y	DF FF EF CD EF	dd hh ll ff ff	4 5 5 6	—	—	—	—	Δ	Δ	0	—
STY (opr)	Store Index Register Y	IY ⇒ M : M + 1	DIR EXT IND,X IND,Y	18 DF 18 FF 1A EF 18 EF	dd hh ll ff ff	5 6 6 6	—	—	—	—	Δ	Δ	0	—
SUBA (opr)	Subtract Memory from A	A – M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	80 90 B0 A0 18 A0	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
SUBB (opr)	Subtract Memory from B	B – M ⇒ B	A IMM A DIR A EXT A IND,X A IND,Y	C0 D0 F0 E0 18 E0	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
SUBD (opr)	Subtract Memory from D	D – M : M + 1 ⇒ D	IMM DIR EXT IND,X IND,Y	83 93 B3 A3 18 A3	jj kk dd hh ll ff ff	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
SWI	Software Interrupt	See Figure 3–2	INH	3F	—	14	—	—	—	1	—	—	—	—
TAB	Transfer A to B	A ⇒ B	INH	16	—	2	—	—	—	—	Δ	Δ	0	—
TAP	Transfer A to CC Register	A ⇒ CCR	INH	06	—	2	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
TBA	Transfer B to A	B ⇒ A	INH	17	—	2	—	—	—	—	Δ	Δ	0	—
TEST	TEST (Only in Test Modes)	Address Bus Counts	INH	00	—	*	—	—	—	—	—	—	—	—
TPA	Transfer CC Register to A	CCR ⇒ A	INH	07	—	2	—	—	—	—	—	—	—	—
TST (opr)	Test for Zero or Minus	M – 0	EXT IND,X IND,Y	7D 6D 18 6D	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	0	0
TSTA	Test A for Zero or Minus	A – 0	A INH	4D	—	2	—	—	—	—	Δ	Δ	0	0
TSTB	Test B for Zero or Minus	B – 0	B INH	5D	—	2	—	—	—	—	Δ	Δ	0	0
TSX	Transfer Stack Pointer to X	SP + 1 ⇒ IX	INH	30	—	3	—	—	—	—	—	—	—	—

Table 1. Instruction Set (Sheet 8 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
TSY	Transfer Stack Pointer to Y	SP + 1 ⇒ IY	INH	18 30	—	4	—	—	—	—	—	—	—	—
TXS	Transfer X to Stack Pointer	IX – 1 ⇒ SP	INH	35	—	3	—	—	—	—	—	—	—	—
TYS	Transfer Y to Stack Pointer	IY – 1 ⇒ SP	INH	18 35	—	4	—	—	—	—	—	—	—	—
WAI	Wait for Interrupt	Stack Regs & WAIT	INH	3E	—	**	—	—	—	—	—	—	—	—
XGDX	Exchange D with X	IX ⇒ D, D ⇒ IX	INH	8F	—	3	—	—	—	—	—	—	—	—
XGDY	Exchange D with Y	IY ⇒ D, D ⇒ IY	INH	18 8F	—	4	—	—	—	—	—	—	—	—

Cycle
- * Infinity or until reset occurs
- ** 12 cycles are used beginning with the opcode fetch. A wait state is entered which remains in effect for an integer number of MPU E-clock cycles (n) until an interrupt is recognized. Finally, two additional cycles are used to fetch the appropriate interrupt vector (14 + n total).

Operands
- dd = 8-bit direct address ($0000–$00FF) (high byte assumed to be $00)
- ff = 8-bit positive offset $00 (0) to $FF (255) (is added to index)
- hh = High-order byte of 16-bit extended address
- ii = One byte of immediate data
- jj = High-order byte of 16-bit immediate data
- kk = Low-order byte of 16-bit immediate data
- ll = Low-order byte of 16-bit extended address
- mm = 8-bit mask (set bits to be affected)
- rr = Signed relative offset $80 (–128) to $7F (+127)
  (offset relative to address following machine code offset byte))

Operators
- ( ) Contents of register shown inside parentheses
- ⇐ Is transferred to
- ⇑ Is pulled from stack
- ⇓ Is pushed onto stack
- • Boolean AND
- \+ Arithmetic addition symbol except where used as inclusive-OR symbol in Boolean formula
- ⊕ Exclusive-OR
- ∗ Multiply
- : Concatenation
- – Arithmetic subtraction symbol or negation symbol (two's complement)

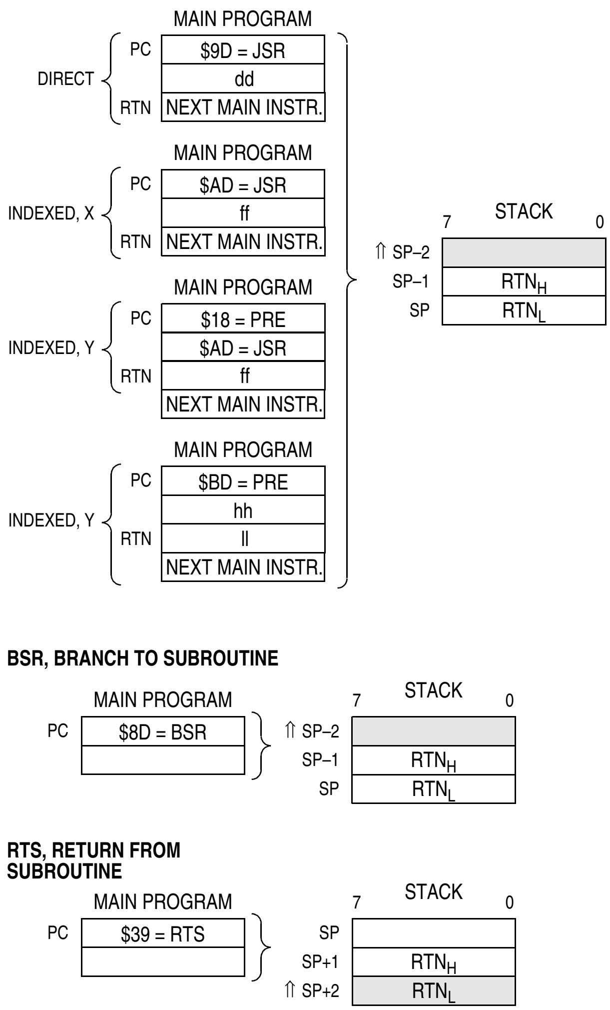
Condition Codes
- — Bit not changed
- 0 Bit always cleared
- 1 Bit always set
- Δ Bit cleared or set, depending on operation
- ↓ Bit can be cleared, cannot become set

Special Operations

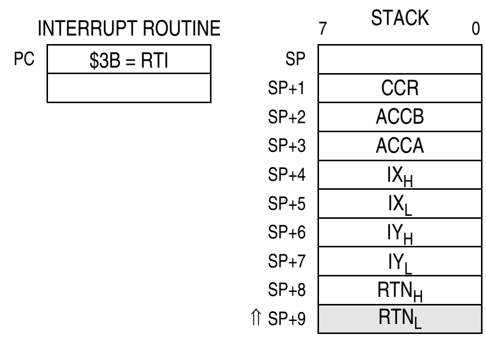
JSR, JUMP TO SUBROUTINE

BSR, BRANCH TO SUBROUTINE

RTS, RETURN FROM SUBROUTINE

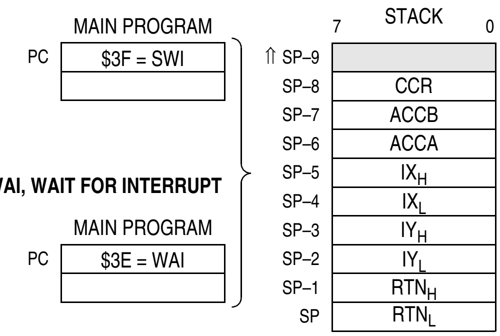


RTI, RETURN FROM INTERRUPT



SWI, SOFTWARE INTERRUPT

WAI, WAIT FOR INTERRUPT



LEGEND:

RTN = ADDRESS OF NEXT INSTRUCTION IN MAIN PROGRAM TO BE EXECUTED UPON RETURN FROM SUBROUTINE
RTN_H = MOST SIGNIFICANT BYTE OF RETURN ADDRESS
RTN_L = LEAST SIGNIFICANT BYTE OF RETURN ADDRESS
⇑ = STACK POINTER POSITION AFTER OPERATION IS COMPLETE
dd = 8-BIT DIRECT ADDRESS ($0000–$00FF) (HIGH BYTE ASSUMED TO BE $00)
ff = 8-BIT POSITIVE OFFSET $00 (0) TO $FF (255) IS ADDED TO INDEX
hh = HIGH-ORDER BYTE OF 16-BIT EXTENDED ADDRESS
ll = LOW-ORDER BYTE OF 16-BIT EXTENDED ADDRESS
rr = SIGNED RELATIVE OFFSET $80 (–128) TO $7F (+127) (OFFSET RELATIVE TO THE ADDRESS FOLLOWING THE MACHINE CODE OFFSET BYTE)

M68HC11E Series Registers

Figure 6 provides a summary of the M68HC11E registers. Note that the 128-byte register block can be remapped to any 4K boundary.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$1000	Port A Data Register (PORTA)	Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Reset:	I	0	0	0	I	I	I	I
$1001	Reserved		R	R	R	R	R	R	R	R
$1002	Parallel I/O Control Register (PIOC)	Read: Write:	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
		Reset:	0	0	0	0	0	U	1	1
$1003	Port C Data Register (PORTC)	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Reset:	Indeterminate after reset							
$1004	Port B Data Register (PORTB)	Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Reset:	0	0	0	0	0	0	0	0
$1005	Port C Latched Register (PORTCL)	Read: Write:	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
		Reset:	Indeterminate after reset							
$1006	Reserved		R	R	R	R	R	R	R	R
$1007	Port C Data Direction Register (DDRC)	Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Reset:	0	0	0	0	0	0	0	0
$1008	Port D Data Register (PORTD)	Read: Write:	0	0	PD5	PD4	PD3	PD2	PD1	PD0
		Reset:	U	U	I	I	I	I	I	I
$1009	Port D Data Direction Register (DDRD)	Read: Write:			DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
		Reset:	0	0	0	0	0	0	0	0
$100A	Port E Data Register (PORTE)	Read: Write:	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
		Reset:	Indeterminate after reset							
$100B	Timer Compare Force Register (CFORC)	Read: Write:	FOC1	FOC2	FOC3	FOC4	FOC5			
		Reset:	0	0	0	0	0	0	0	0

(shaded) = Unimplemented R = Reserved U = Unaffected

I = Indeterminate after reset

Figure 6. Register and Control Bit Assignments (Sheet 1 of 5)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$100C	Output Compare 1 Mask Register (OC1M)	Read: Write:	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3			
		Reset:	0	0	0	0	0	0	0	0
$100D	Output Compare 1 Data Register (OC1D)	Read: Write:	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3			
		Reset:	0	0	0	0	0	0	0	0
$100E	Timer Counter Register High (TCNTH)	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$100F	Timer Counter Register Low (TCNTL)	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$1010	Timer Input Capture 1 Register High (TIC1H)	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	Indeterminate after reset							
$1011	Timer Input Capture 1 Register Low (TIC1L)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Indeterminate after reset							
$1012	Timer Input Capture 2 Register High (TIC2H)	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	Indeterminate after reset							
$1013	TImer Input Capture 2 Register Low (TIC2L)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Indeterminate after reset							
$1014	Timer Input Capture 3 Register High (TIC3H)	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	Indeterminate after reset							
$1015	Timer Input Capture 3 Register Low (TIC3L)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Indeterminate after reset							
$1016	Timer Output Compare 1 Register High (TOC1H)	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$1017	Timer Output Compare 1 Register Low (TOC1L)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$1018	Timer Output Compare 2 Register High (TOC2H)	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$1019	Timer Output Compare 2 Register Low (TOC2L)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1

(shaded) = Unimplemented R = Reserved U = Unaffected

I = Indeterminate after reset

Figure 6. Register and Control Bit Assignments (Sheet 2 of 5)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$101A	Timer Output Compare 3 Register High (TOC3H)	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$101B	Timer Output Compare 3 Register Low (TOC3L)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$101C	Timer Output Compare 4 Register High (TOC4H)	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$101D	Timer Output Compare 4 Register Low (TOC4L)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$101E	Timer Input Capture 4/Output Compare 5 Register High (TI4/O5)	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$101F	Timer Input Capture 4/Output Compare 5 Register Low (TI4/O5)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$1020	Timer Control Register 1 (TCTL1)	Read: Write:	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
		Reset:	0	0	0	0	0	0	0	0
$1021	Timer Control Register 2 (TCTL2)	Read: Write:	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
		Reset:	0	0	0	0	0	0	0	0
$1022	Timer Interrupt Mask 1 Register (TMSK1)	Read: Write:	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
		Reset:	0	0	0	0	0	0	0	0
$1023	Timer Interrupt Flag 1 (TFLG1)	Read: Write:	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
		Reset:	0	0	0	0	0	0	0	0
$1024	Timer Interrupt Mask 2 Register (TMSK2)	Read: Write:	TOI	RTII	PAOVI	PAII			PR1	PR0
		Reset:	0	0	0	0	0	0	0	0
$1025	Timer Interrupt Flag 2 (TFLG2)	Read: Write:	TOF	RTIF	PAOVF	PAIF				
		Reset:	0	0	0	0	0	0	0	0
$1026	Pulse Accumulator Control Register (PACTL)	Read: Write:	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
		Reset:	0	0	0	0	0	0	0	0
$1027	Pulse Accumulator Count Register (PACNT)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Indeterminate after reset							

(shaded) = Unimplemented   R = Reserved   U = Unaffected

I = Indeterminate after reset

Figure 6. Register and Control Bit Assignments (Sheet 3 of 5)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$1028	Serial Peripheral Control Register (SPCR)	Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
		Reset:	0	0	0	0	0	1	U	U
$1029	Serial Peripheral Status Register (SPSR)	Read: Write:	SPIF	WCOL		MODF				
		Reset:	0	0	0	0	0	0	0	0
$102A	Serial Peripheral Data I/O Register (SPDR)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Indeterminate after reset							
$102B	Baud Rate Register (BAUD)	Read: Write:	TCLR	SCP2(1)	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
		Reset:	0	0	0	0	0	U	U	U

1. SCP2 adds ÷ 39 to SCI prescaler and is present only in MC68HC(7)11E20.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$102C	Serial Communications Control Register 1 (SCCR1)	Read: Write:	R8	T8		M	WAKE			
		Reset:	I	I	0	0	0	0	0	0
$102D	Serial Communications Control Register 2 (SCCR2)	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Reset:	0	0	0	0	0	0	0	0
$102E	Serial Communications Status Register (SCSR)	Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	
		Reset:	1	1	0	0	0	0	0	0
$102F	Serial Communications Data Register (SCDR)	Read: Write:	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
		Reset:	Indeterminate after reset							
$1030	Analog-to-Digital Control Status Register (ADCTL)	Read:	CCF		SCAN	MULT	CD	CC	CB	CA
		Write:								
		Reset:	0	0	Indeterminate after reset					
$1031	Analog-to-Digital Results Register 1 (ADR1)	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$1032	Analog-to-Digital Results Register 2 (ADR2)	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$1033	Analog-to-Digital Results Register 3 (ADR3)	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$1034	Analog-to-Digital Results Register 4 (ADR4)	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							

(shaded) = Unimplemented   R = Reserved   U = Unaffected

I = Indeterminate after reset

Figure 6. Register and Control Bit Assignments (Sheet 4 of 5)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$1035	Block Protect Register (BPROT)	Read: Write:				PTCON	BPRT3	BPRT2	BPRT1	BPRT0
		Reset:	0	0	0	1	1	1	1	1
$1036	EPROM Programming Control Register (EPROG)(1)	Read: Write:	MBE		ELAT	EXCOL	EXROW	T1	T0	PGM
		Reset:	0	0	0	0	0	0	0	0

1. MC68HC711E20 only

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$1037	Reserved		R	R	R	R	R	R	R	R
$1038	Reserved		R	R	R	R	R	R	R	R
$1039	System Configuration Options Register (OPTION)	Read: Write:	ADPU	CSEL	IRQE(1)	DLY(1)	CME		CR1(1)	CR0(1)
		Reset:	0	0	0	1	0	0	0	0
$103A	Arm/Reset COP Timer Circuitry Register (COPRST)	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$103B	EPROM and EEPROM Programming Control Register (PPROG)	Read: Write:	ODD	EVEN	ELAT(2)	BYTE	ROW	ERASE	EELAT	EPGM
		Reset:	0	0	0	0	0	0	0	0
$103C	Highest Priority I Bit Interrupt and Miscellaneous Register (HPRIO)	Read: Write:	RBOOT	SMOD	MDA	IRV(NE)	PSEL3	PSEL2	PSEL1	PSEL0
		Reset:	0	0	0	0	0	1	1	0
$103D	RAM and I/O Mapping Register (INIT)	Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
		Reset:	0	0	0	0	0	0	0	1
$103E	Reserved		R	R	R	R	R	R	R	R
$103F	System Configuration Register (CONFIG)	Read: Write:					NOSEC	NOCOP	ROMON	EEON
		Reset:	0	0	0	0	U	U	1	U
$103F	System Configuration Register (CONFIG)(3)	Read: Write:	EE3	EE2	EE1	EE0	NOSEC	NOCOP		EEON
		Reset:	1	1	1	1	U	U	1	1

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time during special modes.
2. MC68HC711E9 only
3. MC68HC811E2 only

[shaded] = Unimplemented R = Reserved U = Unaffected

I = Indeterminate after reset

Figure 6. Register and Control Bit Assignments (Sheet 5 of 5)

A/D Control/Status Register (ADCTL)

Address: $1030

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CCF		SCAN	MULT	CD	CC	CB	CA
Write:								
Reset:	0	0	Indeterminate after reset					

(shaded) = Unimplemented

CCF — Conversion Complete Flag

This bit is set after an A/D conversion cycle and cleared when ADCTL is written.

Bit 6 — Unimplemented

Always reads 0

SCAN — Continuous Scan Control

0 = Do four conversions and stop
1 = Convert four channels in selected group continuously

MULT — Multiple Channel/Single Channel Control

0 = Convert single channel selected
1 = Convert four channels in selected group

CD:CA — Channel Selects D:A

Refer to the following table.

Channel Select Control Bits CD:CC:CB:CA	Channel Signal	Result in ADRx if MULT = 1	Result in ADRx if MULT = 0
0000	AN0	ADR1	ADR[4:1]
0001	AN1	ADR2	ADR[4:1]
0010	AN2	ADR3	ADR[4:1]
0011	AN3	ADR4	ADR[4:1]
0100	AN4	ADR1	ADR[4:1]
0101	AN5	ADR2	ADR[4:1]
0110	AN6	ADR3	ADR[4:1]
0111	AN7	ADR4	ADR[4:1]
10XX	Reserved	—	—
1100	V_{RH}(1)	ADR1	ADR[4:1]
1101	V_{RL}(1)	ADR2	ADR[4:1]
1110	$(V_{RH})/2$(1)	ADR3	ADR[4:1]
1111	Reserved(1)	ADR4	ADR[4:1]

NOTES:
1. Used for factory testing

A/D Results (ADR1–ADR4)

ADR1 — Address: $1031

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	Indeterminate after reset							

ADR2 — Address: $1032

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	Indeterminate after reset							

ADR3 — Address: $1033

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	Indeterminate after reset							

ADR4 — Address: $1034

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	Indeterminate after reset							

(shaded) = Unimplemented

Analog Input to 8-Bit Result Translation Table

	Bit 7	6	5	4	3	2	1	Bit 0
%(1)	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
Volts(2)	2.500	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195
Volts(3)	1.65	8.25	0.4125	0.2063	0.1031	0.0516	0.0258	0.0129

NOTES:
1. % of $V_{RH}–V_{RL}$
2. Voltages for V_{RL} = 0; V_{RH} = 5.0 V
3. Voltages for V_{RL} = 0; V_{RH} = 3.3 V

Baud Rate Control Register (BAUD)

Address: $102B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TCLR	SCP2	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
Reset:	0	0	0	0	0	U	U	U

U = Unaffected

TCLR — Clear Baud Rate Counter (Test)

SCP[2:0] — SCI Baud Rate Prescaler Select

SCP2 applies to the MC68HC(7)11E20 only. When SCP2 = 1, SCP[1:0] must equal 0. Any other values for SCP[1:0] are not decoded in the prescaler and the results are unpredictable.

SCP			Divide Internal Clock By	Crystal Frequency (MHz)				
2(1)	1	0		4.0	4.9152	8.0	8.3886	12.0
0	0	0	1	62500	76800	125000	131072	187500
0	0	1	3	20833	25600	41667	43691	62500
0	1	0	4	15625	19200	31250	32768	46875
0	1	1	13	4800	5907	9600	10082	14423
1	0	0	39	1602	1969	3205	3361	4808

NOTES:
1. Shaded areas apply to MC68HC(7)11E20 only.

RCKB — SCI Baud Rate Clock Check (TEST)

SCR[2:0] — SCI Baud Rate Selects

Selects receiver and transmitter bit rate based on output from baud rate prescaler stage. Refer to SCI baud rate generator block diagram.

SCR			Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table				
2	1	0		131072	76800	32768	19200	4800
0	0	0	1	131072	76800	32768	19200	4800
0	0	1	2	65536	38400	16384	9600	2400
0	1	0	4	32768	19200	8192	4800	1200
0	1	1	8	16384	9600	4096	2400	600
1	0	0	16	8192	480	2048	1200	300
1	0	1	32	4096	2400	1024	600	150
1	1	0	64	2048	1200	512	300	75
1	1	1	128	1024	600	256	150	37.5

Block Protect Register (BPROT)

Address: $1035

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:				PTCON	BPRT3	BPRT2	BPRT1	BPRT0
Reset:	0	0	0	1	1	1	1	1

= Unimplemented

Bits [7:5] — Unimplemented

Always read 0

PTCON — Protect CONFIG Register

0 = CONFIG register can be programmed or erased normally.
1 = CONFIG register cannot be programmed or erased.

BPRT[3:0] — Block Protect for EEPROM

Block protect register bits can be written to 0 (protection disabled) only once within 64 cycles of a reset in normal modes, or at any time in special modes. Block protect register bits can be written to 1 (protection enabled) at any time.

0 = Protection disabled for associated block
1 = Protection enabled for associated block

Bit Name	Block Protected	Block Size
BPRT0	$B600–$B61F	32 bytes
BPRT1	$B620–$B65F	64 bytes
BPRT2	$B660–$B6DF	128 bytes
BPRT3	$B6E0–$B7FF	288 bytes
	MC68HC811E2 Only	
BPRT0	$x800–$x9FF(1)	512 bytes
BPRT1	$xA00–$xBFF(1)	512 bytes
BPRT2	$xC00–$xDFF(1)	512 bytes
BPRT3	$xE00–$xFFF(1)	512 bytes

NOTES:
1. x is determined by the value of EE[3:0] in CONFIG (MC68HC811E2 only). Refer to the MC68HC811E2 CONFIG register.

Timer Compare Force Register (CFORC)

Address: $100B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	FOC1	FOC2	FOC3	FOC4	FOC5			
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

FOC[1:5] — Force Output Comparison

Write 1s to force compare(s).

0 = Not affected

1 = Output x action occurs

Bits [2:0] — Unimplemented

Always read 0

Configuration Register (CONFIG)

Security disable, COP, ROM mapping, and EEPROM enables

Address: $103F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:					NOSEC	NOCOP	ROMON	EEON
Resets:								
Single chip:	0	0	0	0	U	U	1	U
Bootstrap:	0	0	0	0	U	U(L)	U	U
Expanded:	0	0	0	0	1	U	U	U
Test:	0	0	0	0	1	U(L)	U	U

= Unimplemented

U indicates a previously programmed bit. U(L) indicates that the bit resets to the logic level held in the latch prior to reset, but the function of COP is controlled by the DISR bit in TEST1 register.

The following register description applies to the MC68HC11E2 only.

Address: $103F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EE3	EE2	EE1	EE0	NOSEC	NOCOP		EEON
Resets:								
Single chip:	1	1	1	1	U	U	1	1
Bootstrap:	1	1	1	1	U	U(L)	1	1
Expanded:	U	U	U	U	1	U	1	U
Test:	U	U	U	U	1	U(L)	1	0

= Unimplemented

U indicates a previously programmed bit. U(L) indicates that the bit resets to the logic level held in the latch prior to reset, but the function of COP is controlled by the DISR bit in TEST1 register.

EE[3:0] — EEPROM Map Position (MC68HC811E2 only)

EE[3:0] determine the upper four bits of EEPROM address, positioning EEPROM at the selected 4-Kbyte boundary. In single-chip and boot modes, these bits are set to 1s during reset and EEPROM is mapped to top of memory. Not implemented in other E-series devices; always read 0. Refer to the following table.

EE3	EE1	EE2	EE0	EEPROM Location
0	0	0	0	$0800–$0FFF
0	0	0	1	$1800–$1FFF
0	0	1	0	$2800–$2FFF
0	0	1	1	$3800–$3FFF
0	1	0	0	$4800–$4FFF
0	1	0	1	$5800–$5FFF
0	1	1	0	$6800–$6FFF
0	1	1	1	$7800–$7FFF
1	0	0	0	$8800–$8FFF
1	0	0	1	$9800–$9FFF
1	0	1	0	$A800–$AFFF
1	0	1	1	$B800–$BFFF
1	1	0	0	$C800–$CFFF
1	1	0	1	$D800–$DFFF
1	1	1	0	$E800–$EFFF
1	1	1	1	$F800–$FFFF

NOSEC — Security Disable

NOSEC is invalid unless the security mask option is specified before the MCU is manufactured. If the security mask option is omitted NOSEC always reads 1. The enhanced security feature is available in the MC68S711E9 MCU. The enhancement to the standard security feature protects the EPROM as well as RAM and EEPROM.

0 = RAM/EEPROM security mode enabled
1 = RAM/EEPROM security mode disabled

NOCOP — COP System Disable

Resets to programmed value.

0 = COP enabled (forces reset on timeout)
1 = COP disabled (does not force reset on timeout)

ROMON — ROM/EPROM Enable

In single-chip mode, ROMON is forced to 1 out of reset. ROMON does not apply to the MC68HC811E2. For devices with disabled ROM arrays (the MC68HC11E0, MC68HC11E1, MC68L11E0, or MC68L11E1) ROMON must never be set to 1.

0 = ROM/EPROM removed from the memory map
1 = ROM/EPROM present in the memory map

EEON — EEPROM Enable

0 = EEPROM removed from the memory map
1 = EEPROM present in the memory map

Arm/Reset COP Timer Circuitry Register (COPRST)

Address: $103A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	6	5	4	3	2	1	BIT 0
Reset:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism. Write $AA to COPRST to reset COP watchdog.

Data Direction Register for Port C (DDRC)

Address: $1007

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
Reset:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction for Port C

In handshake output mode, DDRC bits selected the three-stated output option (DDCx = 1).

0 = Input
1 = Output

Data Direction Register for Port D (DDRD)

Address: $1009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	(Unimplemented)	(Unimplemented)	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
Reset:	0	0	0	0	0	0	0	0

(shaded) = Unimplemented

Bits [7:6] — Unimplemented

Always read 0

DDD[5:0] — Data Direction for Port D

0 = Input
1 = Output

EPROM Programming Control Register (EPROG)

Address: $1036

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MBE		ELAT	EXCOL	EXROW	T1	T0	PGM
Reset:	0	0	0	0	0	0	0	0

(shaded) = Unimplemented

NOTE

EPROG is present only on the MC68HC711E20.

MBE — Multiple-Byte Programming Enable

When multiple-byte programming is enabled, address bit 5 is considered a don’t care so that bytes with address bit 5 = 0 and address bit 5 = 1 both get programmed. MBE can be read in any mode and always reads 0 in normal modes. MBE can be written only in special modes.

0 = EPROM array configured for normal programming
1 = Program two bytes with the same data

Bit 6 — Unimplemented

Always reads 0

ELAT — EPROM/OTPROM Latch Control

When ELAT = 1, writes to EPROM cause address and data to be latched and the EPROM/OTPROM cannot be read. ELAT can be read any time. ELAT can be written any time except when PGM = 1; then the write to ELAT is disabled.

0 = EPROM/OTPROM address and data bus configured for normal reads
1 = EPROM/OTPROM address and data bus configured for programming

EXCOL — Select Extra Columns

0 = User array selected
1 = User array is disabled and extra columns are accessed at bits [7:0]. Addresses use bits [13:5] and bits [4:0] are don’t care. EXCOL can be read and written only in special modes and always returns 0 in normal modes.

EXROW — Select Extra Rows

0 = User array selected
1 = User array is disabled and two extra rows are available. Addresses use bits [7:0] and bits [13:8] are don’t care. EXROW can be read and written only in special modes and always returns 0 in normal modes.

T[1:0] — EPROM Test Mode Select

These bits allow selection of either gate stress or drain stress test modes. They can be read and written only in special modes and always read 0 in normal modes.

T1	T0	Function Selected
0	0	Normal mode
0	1	Reserved
1	0	Gate stress
1	1	Drain stress

PGM — EPROM Programming Voltage Enable

PGM can be read any time and can be written only when ELAT = 1.
0 = Programming voltage to EPROM array disconnected
1 = Programming voltage to EPROM array connected

Highest Priority I Bit Interrupt and Miscellaneous (HPRIO)

Address: $103C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RBOOT(1)	SMOD(1)	MDA(1)	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
Reset:								
Single chip:	0	0	0	0	0	1	1	0
Expanded:	0	0	1	0	0	1	1	0
Bootstrap:	1	1	0	0	0	1	1	0
Special test:	0	1	1	1	0	1	1	0

1. The values of the RBOOT, SMOD, and MDA reset bits depend on the mode selected at the $\overline{\text{RESET}}$ pin rising edge.

RBOOT — Read Bootstrap ROM

Valid only when SMOD is set to 1 (bootstrap or special test mode). Can only be written in special modes.
0 = Bootloader ROM disabled and not in map
1 = Bootloader ROM enabled and in map at $BE00–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

The initial value of SMOD is in the **inverse** of the logic level present on the MODB pin at the rising edge of reset. The initial value of MDA equals the logic level present on the MODA pin at the rising edge of reset. These two bits can be read at any time. They can be written anytime in special modes. MDA can only be written once in normal modes. SMOD cannot be set once it has been cleared. Refer to the following table.

Inputs		Mode	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single chip	0	0
1	1	Expanded	0	1
0	0	Bootstrap	1	0
0	1	Special test	1	1

IRVNE — Internal Read Visibility/Not E (IRV in MC68HC811E2)

IRVNE can be written once in any mode. In expanded modes, IRVNE determines whether IRV is on or off. In special test mode, IRVNE is reset to 1. For the MC68HC811E2, this bit controls only internal read visibility function and has no meaning or effect in single-chip modes.

0 = No internal read visibility on external bus
1 = Data from internal reads is driven out the external data bus

In single-chip modes this bit determines whether the E clock drives out from the chip.

0 = E is driven out from the chip.
1 = E pin is driven low. Refer to the following table.

Mode	IRVNE Out of Reset	E Clock Out of Reset	IRV Out of Reset	IRVNE Affects Only	IRVNE Can Be Written
Single chip	0	On	Off	E	Once
Expanded	0	On	Off	IRV	Once
Bootstrap	0	On	Off	E	Once
Special test	1	On	On	IRV	Once

NOTE

When IRV function is used, care must be taken to ensure that bus conflicts do not occur. Data can be driven onto the bus even though the $R/\overline{W}$ line indicates a high-impedance state on data bus pins.

PSEL[3:0] — Priority Select

Can be written only while bit I in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I bit related sources. Refer to the following table.

PSEL3	PSEL2	PSEL1	PSEL0	Interrupt Source Promoted
0	0	0	0	Timer overflow
0	0	0	1	Pulse accumulator overflow
0	0	1	0	Pulse accumulator input edge
0	0	1	1	SPI serial transfer complete
0	1	0	0	SCI serial system
0	1	0	1	Reserved (default to $\overline{IRQ}$)
0	1	1	0	$\overline{IRQ}$ (external pin or parallel I/O)
0	1	1	1	Real-time interrupt
1	0	0	0	Timer input capture 1
1	0	0	1	Timer input capture 2
1	0	1	0	Timer input capture 3
1	0	1	1	Timer output compare 1
1	1	0	0	Timer output compare 2
1	1	0	1	Timer output compare 3
1	1	1	0	Timer output compare 4
1	1	1	1	Timer input capture 4/output compare 5

RAM and Register Mapping (INIT)

Address: $103D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
Reset:	0	0	0	0	0	0	0	1

RAM[3:0] — Internal RAM Map Position

Determine the upper four bits of RAM address. At reset, RAM is mapped to $0000.

RAM[3:0]	Address	RAM[3:0]	Address
0000	$0000–$0xFF	1000	$8000–$8xFF
0001	$1000–$1xFF	1001	$9000–$9xFF
0010	$2000–$2xFF	1010	$A000–$AxFF
0011	$3000–$3xFF	1011	$B000–$BxFF
0100	$4000–$4xFF	1100	$C000–$CxFF
0101	$5000–$5xFF	1101	$D000–$DxFF
0110	$6000–$6xFF	1110	$E000–$ExFF
0111	$7000–$7xFF	1111	$F000–$FxFF

REG[3:0] — 64-Byte Register Block Map Position

Determine upper four bits of register space address. At reset, registers are mapped to $1000.

REG[3:0]	Address	REG[3:0]	Address
0000	$0000–$003F	1000	$8000–$803F
0001	$1000–$103F	1001	$9000–$903F
0010	$2000–$203F	1010	$A000–$A03F
0011	$3000–$303F	1011	$B000–$B03F
0100	$4000–$403F	1100	$C000–$C03F
0101	$5000–$503F	1101	$D000–$D03F
0110	$6000–$603F	1110	$E000–$E03F
0111	$7000–$703F	1111	$F000–$F03F

NOTE

Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes.

Output Compare 1 Data Register (OC1D)

Address: $100D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3			
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits [2:0]— Unimplemented

Always reads 0

Output Compare 1 Mask Register (OC1M)

Address: $100C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3			
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

OC1M[7:3] — Output Compare Masks

0 = OC1 disabled

1 = OC1 enabled to control the corresponding pin of port A

Bits [2:0]— Unimplemented

Always reads 0

System Configuration Options (OPTION)

Address: $1039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE(1)	DLY(1)	CME		CR1(1)	CR0(1)
Reset:	0	0	0	1	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time during special modes.

= Unimplemented

ADPU — Analog-to-Digital (A/D) Converter Power-Up

0 = A/D powered down
1 = A/D powered up

CSEL — Clock Select

0 = A/D and EEPROM charge pumps use system E clock
1 = A/D and EEPROM charge pumps use internal RC oscillator

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only

0 = Low level recognition
1 = Falling edge recognition

DLY — Enable Oscillator Startup Delay on Exit from Stop Mode

0 = No stabilization delay on exit from stop mode
1 = Stabilization delay enabled on exit from stop mode

CME — Clock Monitor Enable

0 = Clock monitor disabled; slow clocks can be used
1 = Slow or stopped clocks cause clock failure reset

Bit 2 — Not implemented

Always reads 0

CR[1:0] — COP Timer Rate Select

Refer to the following table.

CR[1:0]	Divide $E/2^{15}$ By	XTAL = 4.0 MHz Timeout – 0 ms, + 32.8 ms	XTAL = 8.0 MHz Timeout – 0 ms, + 16.4 ms	XTAL = 12.0 MHz Timeout – 0 ms, + 10.9 ms	XTAL = 16.0 MHz Timeout – 0 ms, + 8.2 ms
0 0	1	32.768 ms	16.384 ms	10.923 ms	8.19 ms
0 1	4	131.072 ms	65.536 ms	43.691 ms	32.8 ms
1 0	16	524.28 ms	262.14 ms	174.76 ms	131 ms
1 1	64	2.098 s	1.049 s	699.05 ms	524 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz	4.0 MHz

Pulse Accumulator Counter (PACNT)

Address: $1027

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	6	5	4	3	2	1	BIT 0
Reset:	Unaffected by reset							

Pulse Accumulator Control (PACTL)

Address: $1026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
Reset:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7

0 = Input only
1 = Output

PAEN — Pulse Accumulator System Enable

0 = Pulse accumulator disabled
1 = Pulse accumulator enabled

PAMOD — Pulse Accumulator Mode

0 = Event counter
1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control

Refer to the following table.

PAMOD	PEDGE	Action on Clock
0	0	PAI falling edge increments the counter.
0	1	PAI rising edge increments the counter.
1	0	A zero on PAI inhibits counting.
1	1	A one on PAI inhibits counting.

DDRA3 — Data Direction for Port A Bit 3

Overridden if an output compare function is configured to control the PA3 pin.

0 = Input
1 = Output

I4/O5 — Input Capture 4/Output Compare 5

Configure TI4/O5 for input capture or output compare

0 = OC5 enabled
1 = IC4 enabled

RTR[1:0] — Real-Time Interrupt (RTI) Rate

Refer to the following table.

RTR1	RTR0	E = 3 MHz	E = 2 MHz	E = 1 MHz	E = X MHz
0	0	2.731 ms	4.096 ms	8.192 ms	$(E/2^{13})$
0	1	5.461 ms	8.192 ms	16.384 ms	$(E/2^{14})$
1	0	10.923 ms	16.384 ms	32.768 ms	$(E/2^{15})$
1	1	21.845 ms	32.768 ms	65.536 ms	$(E/2^{16})$

Parallel I/O Control (PIOC)

Address: $1002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
Reset:	0	0	0	0	0	U	1	1

U = Unaffected

STAF — Strobe A Interrupt Status Flag

STAF is set when the selected edge occurs on strobe A. This bit can be cleared by a read of PIOC with STAF set followed by a read of PORTCL (simple strobed or full input handshake mode) or a write to PORTCL (output handshake mode).

0 = No active edge detected
1 = Selected active edge detected

STAI — Strobe A Interrupt Enable Mask

0 = STAF does not request interrupt
1 = STAF requests interrupt

CWOM — Port C Wired-OR Mode (affects all eight port C pins)

0 = Port C outputs are normal CMOS outputs.
1 = Port C outputs are open-drain outputs.

HNDS — Handshake Mode Bit

0 = Simple strobe mode
1 = Full input or output handshake mode

OIN — Output or Input Handshake Select

HNDS must be set to 1 for this bit to have meaning.

0 = Input handshake
1 = Output handshake

PLS — Pulsed/Interlocked Handshake Operation

HNDS must be set to 1 for this bit to have meaning. When interlocked handshake is selected, strobe B is active until the selected edge of strobe A is detected.

0 = Interlocked handshake
1 = Pulsed handshake (Strobe B pulses high for two E-clock cycles.)

EGA — Active Edge for Strobe A

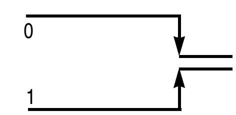
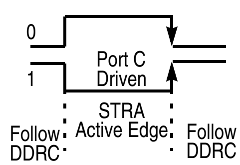
0 = STRA falling edge selected

1 = STRA rising edge selected

INVB — Invert Strobe B

0 = Active level is logic 0.

1 = Active level is logic 1.

	STAF Clearing Sequence	HNDS	OIN	PLS	EGA	Port B	Port C
Simple strobed mode	Read PIOC with STAF = 1 then read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA	STRB pulses on writes to PORTB
Full-input hand-shake mode	Read PIOC with STAF = 1 then read PORTCL	1	0	0 = STRB active level 1 = STRB active pulse		Inputs latched into PORTCL on any active edge on STRA	Normal output port, unaffected in handshake modes
Full-output hand-shake mode	Read PIOC with STAF = 1 then write PORTCL	1	1	0 = STRB active level 1 = STRB active pulse		Driven as outputs if STRA at active level; follows DDRC if STRA not at active level	Normal output port, unaffected in handshake modes

Port A Data Register (PORTA)

Address: $1000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset:	I	0	0	0	I	I	I	I
Alt. Pin Function:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/OR	OC1	OC1	OC1	OC1	OC1	—	—	—

NOTE

I/O pins configured as high-impedance inputs have port data that is indeterminate. The contents of the corresponding latches are dependent upon the electrical state of the pins during reset. This is indicated by an "I" in the port description.

Port B Data Register (PORTB)

Address: $1004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB2	PB0
Reset:	0	0	0	0	0	0	0	0
Single Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Expanded or Test:	ADDR15	ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8

Port C Data Register (PORTC)

Address: $1003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC2	PC0
Reset:	0	0	0	0	0	0	0	0
Single Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Expanded or Test:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Port C Latched Data Register (PORTCL)

Address: $1005

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
Reset:	Indeterminate after reset							

Port D Data Register (PORTD)

Address: $1008

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:			PD5	PD4	PD3	PD2	PD1	PD0
Reset:	0	0	I	I	I	I	I	I
Alt. Pin Function	—	—	$\overline{SS}$	SCK	SDO/MOSI	SDI/MISO	TxD	RxD

= Unimplemented

Port E Data Register (PORTE)

Address: $100A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PE7	PE6	PD5	PE4	PE3	PE2	PE1	PE0
Reset:	I	I	I	I	I	I	I	I
Alt. Pin Function	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

EEPROM Programming Control Register (PPROG)

Address: $103B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ODD	EVEN	ELAT[(1)]	BYTE	ROW	ERASE	EELAT	EPGM
Reset:	0	0	0	0	0	0	0	0

1. MC68HC711E9 and MC68S711E9 only

ODD — Program Odd Rows in Half of EEPROM (TEST)

EVEN — Program Even Rows in Half of EEPROM (Test) Bit

ELAT — EPROM/OTPROM Latch Control

Implemented on MC68HC711E9 only

0 = EPROM/OTPROM address and data bus configured for normal reads and cannot be programmed

1 = EPROM/OTPROM address and data bus configured for programming and cannot be read

BYTE — Byte/Other EEPROM Erase Mode

0 = Row or bulk erase mode used

1 = Erase only one byte of EEPROM

ROW — Row/All EEPROM Erase Mode

Only valid when BYTE = 0

0 = Erase all of EEPROM

1 = Erase only one 16-byte row of EEPROM

BYTE	ROW	Action
0	0	Bulk erase (all bytes)
0	1	Row erase (16 bytes)
1	0	Byte erase
1	1	Byte erase

ERASE — Erase/Normal Control for EEPROM

0 = Normal read or program mode

1 = Erase mode

EELAT — EEPROM Latch Control

0 = EEPROM address and data bus configured for normal reads

1 = EEPROM address and data bus configured for programming or erasing

EPGM —EPROM/EEPROM Programming Voltage Enable

0 = Programming voltage to array disconnected (EEPROM only on MC68HC(7)11E20)

1 = Programming voltage to array connected (EEPROM only on MC68HC(7)11E20)

Serial Communication Interface Control Register 1 (SCCR1)

Address: $102C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	R8	T8		M				
Reset:	I	I	0	0	0	0	0	0

(shaded) = Unimplemented

R8 — Receive Data Bit 8

0 = SCI receiver configured for 8-bit data characters.
1 = If M bit is set, R8 stores the ninth data bit in the receive data character.

T8 — Transmit Data Bit 8

0 = SCI transmitter configured for 8-bit data characters.
1 = If M bit is set, R8 stores the ninth data bit in the transmit data character.

Bit 5 — Unimplemented

Always reads 0

M — Mode Bit (select character format)

0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup by Address Mark/Idle

0 = Wakeup by IDLE line recognition
1 = Wakeup by address mark (most significant data bit set)

Bits [2:0] — Unimplemented

Always read 0

Serial Communications Interface Control Register 2 (SCCR2)

Address: $102D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle-Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable
0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wakeup Control
0 = Normal SCI receiver
1 = Wakeup enabled and receiver interrupts inhibited

SBK — Send Break
0 = Break generator off
1 = Break codes generated as long as SBK = 1

Serial Communications Interface Data Register (SCDR)

Address: $102F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
Reset:	I	I	I	I	I	I	I	I

R[7:0]/T[7:0] — Receiver/Transmitter Data Bits [7:0]

Receive and transmit are double buffered. Reads access the receive data buffer, and writes access the transmit data buffer. When the M bit in SCCR1 is set, R8 and T8 in SCCR1 store the ninth bit in receive and transmit data characters.

Serial Communications Interface Status Register (SCSR)

Address: $102E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	
Reset:	1	1	0	0	0	0	0	0

(shaded) = Unimplemented

TDRE — Transmit Data Register Empty Flag

This flag is set when SCDR is empty. Clear the TDRE flag by reading SCSR with TDRE set and then writing to SCDR.

0 = SCDR busy
1 = SCDR empty

TC — Transmit Complete Flag

This flag is set when the transmitter is idle (no data, preamble, or break transmission in progress). Clear the TC flag by reading SCSR with TC set and then writing to SCDR.

0 = Transmitter busy
1 = Transmitter idle

RDRF — Receive Data Register Full Flag

This flag is set if a received character is ready to be read from SCDR. Clear the RDRF flag by reading SCSR with RDRF set and then reading SCDR.

0 = SCDR empty
1 = SCDR full

IDLE — Idle Line Detected Flag

This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR with IDLE set and then reading SCDR.

0 = RxD line active
1 = RxD line idle

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR with OR set and then reading SCDR.

0 = No overrun
1 = Overrun detected

NF — Noise Error Flag

NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR with NF set and then reading SCDR.

0 = Unanimous decision
1 = Noise detected

FE — Framing Error Flag

FE is set when a 0 is detected where a stop bit was expected. Clear the FE flag by reading SCSR with FE set and then reading SCDR.

0 = Stop bit detected
1 = Zero detected

Bit 0 — Unimplemented

Always reads 0

Serial Peripheral Interface Control Register (SPCR)

Address: $1028

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
Reset:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable

0 = SPI interrupts disabled
1 = SPI interrupts enabled

SPE — Serial Peripheral System Enable

0 = SPI off
1 = SPI on

DWOM — Port D Wired-OR Mode Option for Port D Pins PD[5:0]

0 = Normal CMOS outputs
1 = Open-drain outputs

MSTR — Master Mode Select

0 = Slave mode
1 = Master mode

CPOL, CPHA — Clock Polarity, Clock Phase

Refer to Figure 7

SPR[1:0] — SPI Clock Rate Select

See the following table.

SPR1	SPR0	Divide E Clock By	Frequency at E = 1 MHz (Baud)	Frequency at E = 2 MHz (Baud)	Frequency at E = 3 MHz (Baud)	Frequency at E = 4 MHz (Baud)
0	0	2	500 kHz	1.0 MHz	1.5 MHz	2 MHz
0	1	4	250 kHz	500 kHz	750 kHz	1 MHz
1	0	16	62.5 kHz	125 kHz	187.5 kHz	250 kHz
1	1	32	31.3 kHz	62.5 kHz	93.8 kHz	125 kHz

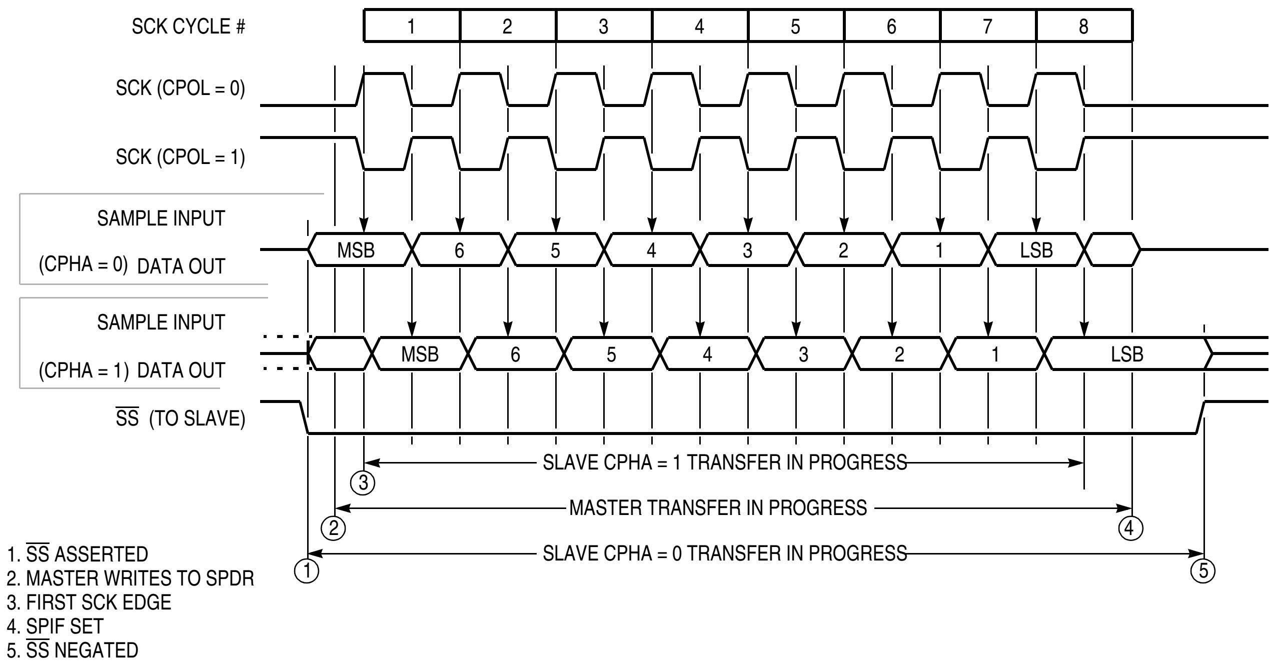


Figure 7. Serial Peripheral Interface Transfer Format

Serial Peripheral Interface Data Register (SPDR)

Address: $102A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	6	5	4	3	2	1	BIT 0

SPI is double buffered in, single buffered out.

Serial Peripheral Interface Status Register (SPSR)

Address: $1029

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIF	WCOL		MODF				
Reset:	0	0	0	0	0	1	U	U

(shaded) = Unimplemented

SPIF — SPI Transfer Complete Flag

This flag is set when an SPI transfer is complete (after eight SCK cycles in a data transfer). Clear this flag by reading SPSR (with SPIF = 1), then access SPDR.

0 = No SPI transfer complete or SPI transfer still in progress
1 = SPI transfer complete

WCOL — Write Collision

This flag is set if the MCU tries to write data into SPDR while an SPI data transfer is in progress. Clear this flag by reading SPSR (with WCOL = 1), then access SPDR.

0 = No write collision error
1 = SPDR written while SPI transfer in progress

Bit 5 — Unimplemented

Always reads 0

MODF — Mode Fault (Mode fault terminates SPI operation)

MODF is set when $\overline{SS}$ is pulled low while MSTR = 1. Clear this flag by reading SPCR with MODF set, then write to SPCR.

0 = No mode fault error
1 = $\overline{SS}$ pulled low in master mode

Bits [3:0] — Unimplemented

Always reads 0

Timer Count Register (TCNT)

Address: $100E — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BIT 15	14	13	12	11	10	9	BIT 8
Write:								
Reset:	0	0	0	0	0	0	0	0

Address: $100F — Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BIT 7	6	5	4	3	2	1	BIT 0
Write:								
Reset:	0	0	0	0	0	0	0	0

(shaded) = Unimplemeted

In normal modes, TCNT is a read-only register.

Timer Control Register 1 (TCTL1)

Address: $1020

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
Reset:	0	0	0	0	0	0	0	0

OM[2:5] — Output Mode

OL[2:5] — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to 0
1	1	Set OCx output line to 1

Timer Control Register 2 (TCTL2)

Address: $1021

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG1B	EDG3B	EDG3A
Reset:	0	0	0	0	0	0	0	0

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

Factory Test Register (TEST1)

Address: $103E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON
Reset:	0	0	0	0	—	0	0	0

(shaded) = Unimplemented

TILOP — Test Illegal Opcode (Test modes only)

Bit 6 — Unimplemented

Always reads 0

OCCR — Output Condition Code Register to Timer Port (Test modes only)

CBYP — Timer Divider Chain Bypass (Test modes only)

DISR — Disable Reset from COP and Clock Monitor (Special modes only (SMOD = 1))

FCM — Force Clock Monitor Failure (Test modes only)

FCOP — Force COP Watchdog Failure (Test modes only)

TCON — Test Configuration (Test modes only)

Timer Interrupt Flag 1 Register (TFLG1)

Address: $1023

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1F	OC2F	OC3F	OC4F	IR/O5F	IC1F	1C2F	IC3F
Reset:	0	0	0	0	0	0	0	0

Clear flags by writing a 1 to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag

Set each time the counter matches output compare x value.

I4/O5F — Input Capture 4/Output Compare 5 Flag

Set by IC4 or OC5, depending on which function was enabled by I4/O5 of PACTL.

IC1F–IC3F — Input Capture x Flag

Set each time a selected active edge is detected on the ICx input line.

Timer Interrupt Flag 2 Register (TFLG2)

Address: $1025

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOF	RTIF	PAOVF	PAIF				
Reset:	0	0	0	0	0	0	0	0

(shaded) = Unimplemented

Clear flags by writing a 1 to the corresponding bit position(s).

TOF — Timer Overflow Flag

Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time (Periodic) Interrupt Flag

The RTIF status bit is automatically set to 1 at the end of every RTI period. To clear RTIF, write a byte to TFLG2 with bit 6 set.

PAOVF — Pulse Accumulator Overflow Flag

Set when PACNT changes from $FF to $00

PAIF — Pulse Accumulator Input Edge Flag

Set each time a selected active edge is detected on the PAI input line.

Bits [3:0] — Unimplemented

Always reads 0

Timer Input Capture 4/Output Compare 5 Register (TI4/O5)

Address: $101E — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	1	1	1	1	1	1	1	1

Address: $101F — Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	1	1	1	1	1	1	1	1

Timer Input Capture Registers (TIC1–TIC3)

TIC1 — Address: $1010 — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	Unaffected by reset							

Address: $1011 — Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	Unaffected by reset							

TIC2 — Address: $1012 — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	Unaffected by reset							

Address: $1013 — Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	Unaffected by reset							

TIC3 — Address: $1014 — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	Unaffected by reset							

Address: $1015 — Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	Unaffected by reset							

Timer Interrupt Mask Register 1 (TMSK1)

Address: $1022

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
Reset:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare x Interrupt Enable

If the OCxI enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

I4/O5I — Input Capture 4/Output Compare 5 Interrupt Enable

When I4/O5 in PACTL is 1, I4/O5I is the input capture 4 interrupt enable bit. When I4/O5 in PACTL is 0, I4/O5I is the output compare 5 interrupt enable bit.

IC1I–IC3I — Input Capture x Interrupt Enable

If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

Timer Interrupt Mask Register 2 (TMSK2)

Address: $1024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII			PR1	PR0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

TOI — Timer Overflow Interrupt Enable

0 = TOF interrupts disabled
1 = Interrupt requested when TOF is set to 1

RTII — Real-Time Interrupt Enable

0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF is set to 1

PAOVI — Pulse Accumulator Input Edge Interrupt Enable

0 = PAOVF interrupts disabled
1 = Interrupt requested when PAOVF is set to 1

PAII — Pulse Accumulator Input Edge Interrupt Enable

0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF is set to 1

Bits [3:2] — Unimplemented

Always reads 0

PR[1:0] — Timer Prescaler Select

In normal modes, PR1 and PR0 can only be written once, and the write must occur within 64 cycles after reset.

PR1	PR0	Prescaler
0	0	÷ 1
0	1	÷ 4
1	0	÷ 8
1	1	÷ 16

Timer Output Compare Registers (TOC1–TOC4)

TOC1 — Address: $1016 — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	1	1	1	1	1	1	1	1

Address: $1017 — Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	1	1	1	1	1	1	1	1

TOC2 — Address: $1018 — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	1	1	1	1	1	1	1	1

Address: $1019 — Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	1	1	1	1	1	1	1	1

TOC3 — Address: $101A — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	1	1	1	1	1	1	1	1

Address: $101B — Low

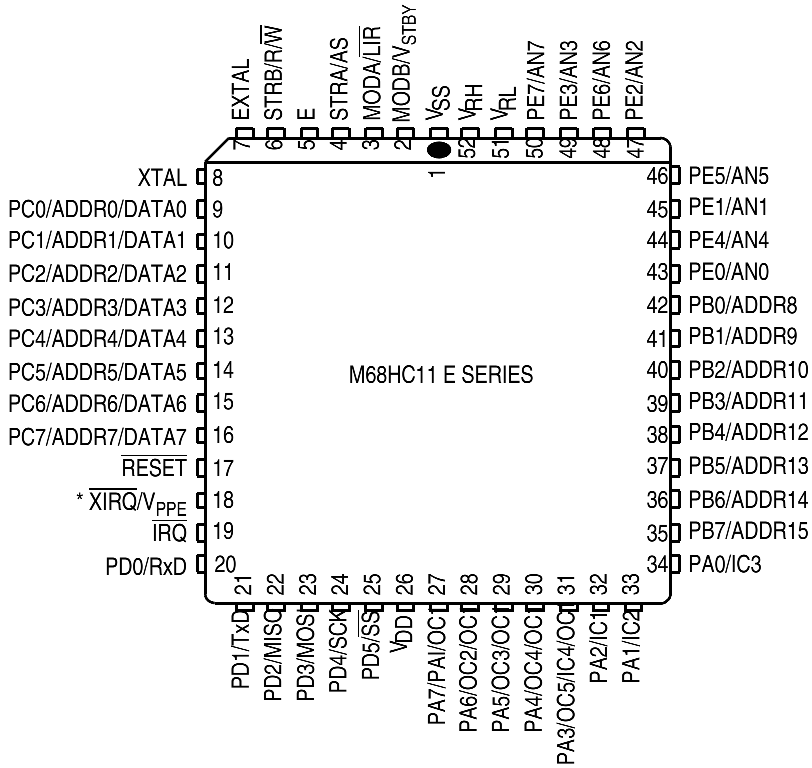
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	1	1	1	1	1	1	1	1

TOC4 — Address: $101C — High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	1	1	1	1	1	1	1	1

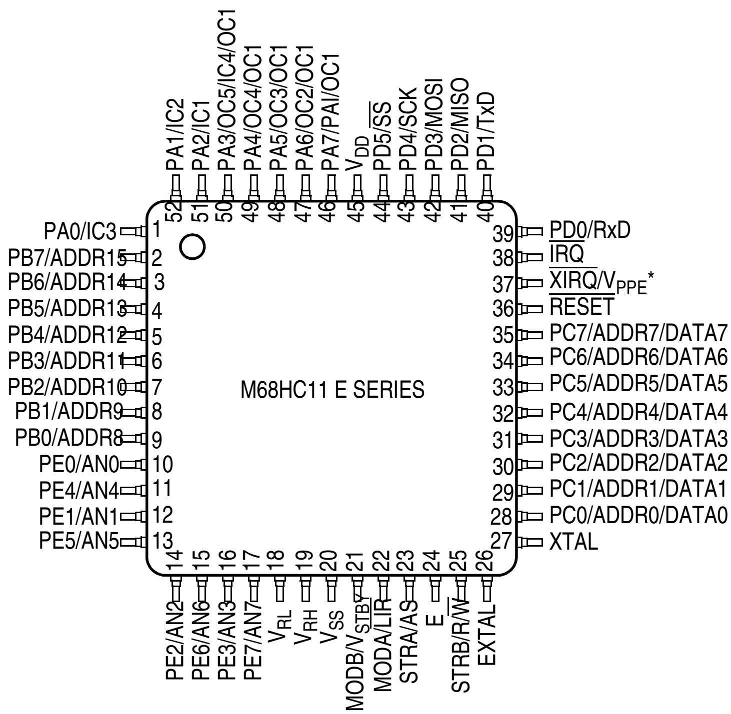
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	1	1	1	1	1	1	1	1

M68HC11 E Series Pin Assignments



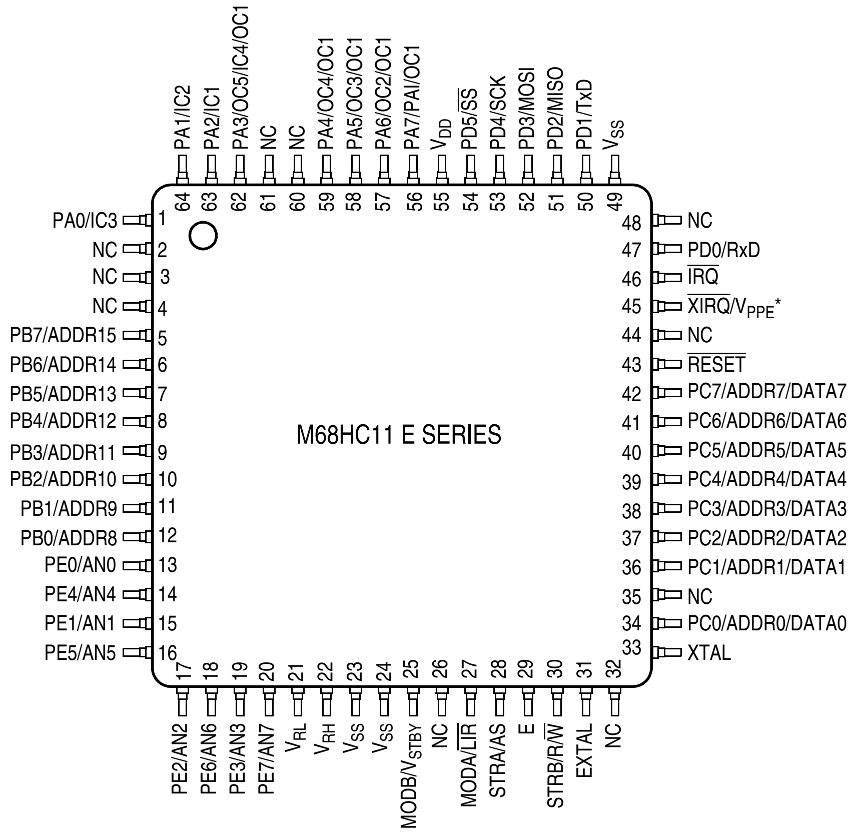
* V_{PPE} applies only to devices with EPROM/OTPROM.

Figure 1. Pin Assignments for 52-Pin PLCC and CLCC



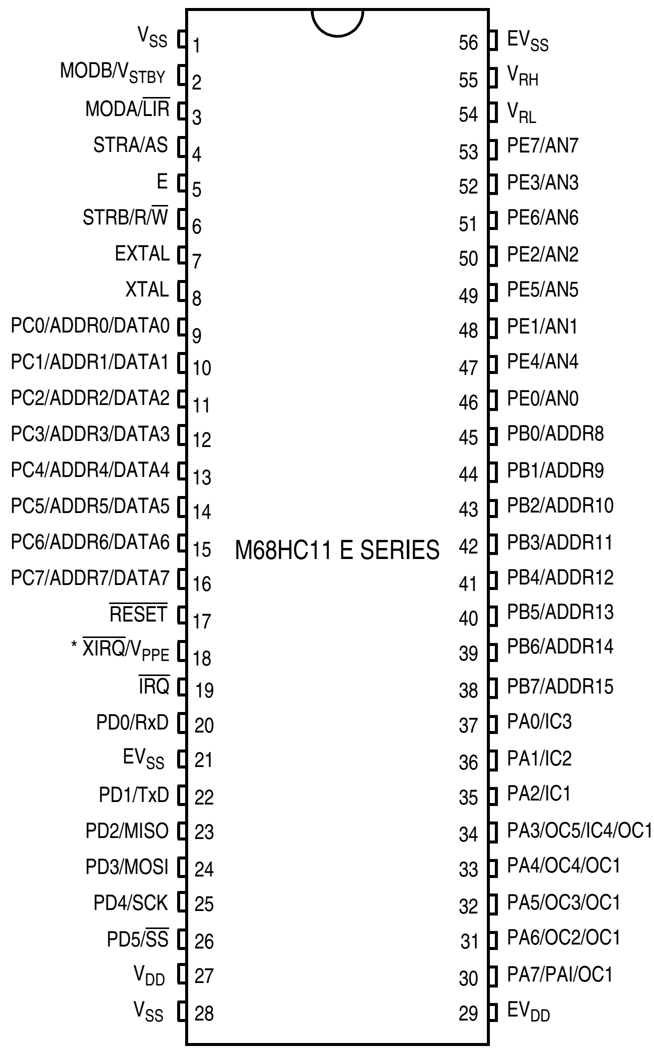
* V_{PPE} applies only to devices with EPROM/OTPROM.

Figure 2. Pin Assignments for 52-Pin TQFP



* V_{PPE} applies only to devices with EPROM/OTPROM.

Figure 3. Pin Assignments for 64-Pin QFP



* V_{PPE} applies only to devices with EPROM/OTPROM.

Figure 4. Pin Assignments for 56-Pin SDIP

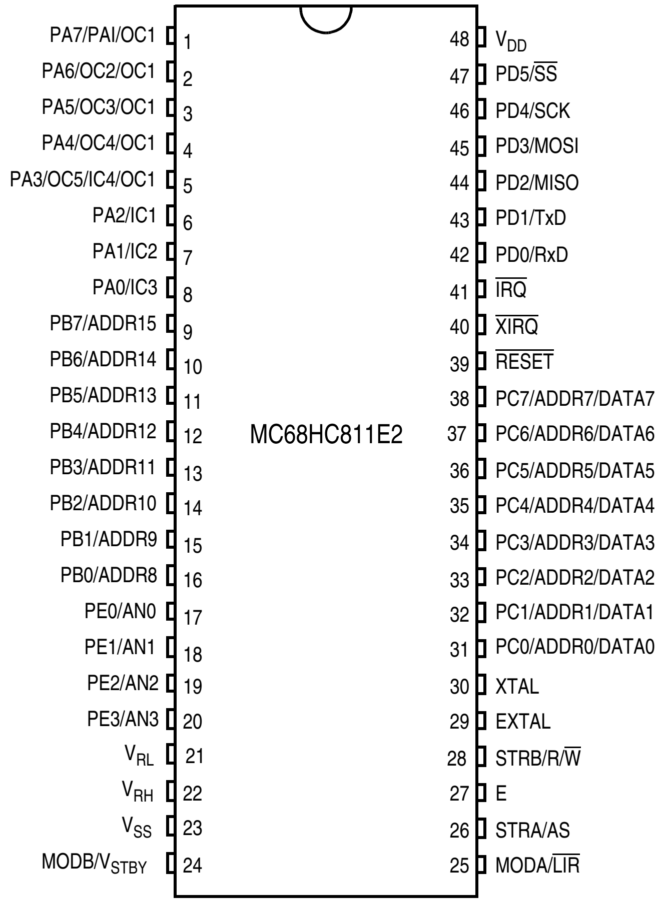


Figure 5. Pin Assignments for 48-Pin DIP (MC68HC811E2)

Conversion Tables

Hexadecimal to ASCII Conversion

Table 2. Hexadecimal to ASCII Conversion

Hex	ASCII	Hex	ASCII	Hex	ASCII	Hex	ASCII
$00	NUL	$20	SP *space*	$40	@	$60	` *grave*
$01	SOH	$21	!	$41	A	$61	a
$02	STX	$22	" quote	$42	B	$62	b
$03	ETX	$23	#	$43	C	$63	c
$04	EOT	$24	$	$44	D	$64	d
$05	ENQ	$25	%	$45	E	$65	e
$06	ACK	$26	&	$46	F	$66	f
$07	BEL *beep*	$27	' *apost.*	$47	G	$67	g
$08	BS *back sp*	$28	(	$48	H	$68	h
$09	HT *tab*	$29	)	$49	I	$69	i
$0A	LF *linefeed*	$2A	*	$4A	J	$6A	j
$0B	VT	$2B	+	$4B	K	$6B	k
$0C	FF	$2C	, *comma*	$4C	L	$6C	l
$0D	CR *return*	$2D	- *dash*	$4D	M	$6D	m
$0E	SO	$2E	. *period*	$4E	N	$6E	n
$0F	SI	$2F	/	$4F	O	$6F	o
$10	DLE	$30	0	$50	P	$70	p
$11	DC1	$31	1	$51	Q	$71	q
$12	DC2	$32	2	$52	R	$72	r
$13	DC3	$33	3	$53	S	$73	s
$14	DC4	$34	4	$54	T	$74	t
$15	NAK	$35	5	$55	U	$75	u
$16	SYN	$36	6	$56	V	$76	v
$17	ETB	$37	7	$57	W	$77	w
$18	CAN	$38	8	$58	X	$78	x
$19	EM	$39	9	$59	Y	$79	y
$1A	SUB	$3A	:	$5A	Z	$7A	z
$1B	ESCAPE	$3B	;	$5B	[	$7B	{
$1C	FS	$3C	<	$5C	\	$7C	|
$1D	GS	$3D	=	$5D	]	$7D	}
$1E	RS	$3E	>	$5E	^	$7E	~
$1F	US	$3F	?	$5F	_ *under*	$7F	DEL *delete*

Hexadecimal to Decimal Conversion

To convert a hexadecimal number (up to four hexadecimal digits) to decimal, look up the decimal equivalent of each hexadecimal digit in Table 3. The decimal equivalent of the original hexadecimal number is the sum of the weights found in the table for all hexadecimal digits.

Table 3. Hexadecimal to/from Decimal Conversion

15Bit8				7Bit0			
1512		118		74		30	
4th Hex Digit		3rd Hex Digit		2nd Hex Digit		1st Hex Digit	
Hex	**Decimal**	**Hex**	**Decimal**	**Hex**	**Decimal**	**Hex**	**Decimal**
0	0	0	0	0	0	0	0
1	4,096	1	256	1	16	1	1
2	8,192	2	512	2	32	2	2
3	12,288	3	768	3	48	3	3
4	16,384	4	1,024	4	64	4	4
5	20,480	5	1,280	5	80	5	5
6	24,576	6	1,536	6	96	6	6
7	28,672	7	1,792	7	112	7	7
8	32,768	8	2,048	8	128	8	8
9	36,864	9	2,304	9	144	9	9
A	40,960	A	2,560	A	160	A	10
B	45,056	B	2,816	B	176	B	11
C	49,152	C	3,072	C	192	C	12
D	53,248	D	3,328	D	208	D	13
E	57,344	E	3,484	E	224	E	14
F	61,440	F	3,840	F	240	F	15

Decimal to Hexadecimal Conversion

To convert a decimal number (up to $65{,}535_{10}$) to hexadecimal, find the largest decimal number in Table 3 that is less than or equal to the number you are converting. The corresponding hexadecimal digit is the most significant hexadecimal digit of the result. Subtract the decimal number found from the original decimal number to get the *remaining decimal value*. Repeat the procedure using the remaining decimal value for each subsequent hexadecimal digit.

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