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Using the HCS12 D family as a development platform for the HCS12 B familiy

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Introduction

The HCS12 D family can be used to emulate the more cost effective B family before it and its associated tool sets become available. As the B family is effectively a sub-set of the D family (with reduced peripheral count) it's possible to use a D family device as an emulation tool in order to develop B family based applications now. This will allow a fast time to market for B family designs when the appropriate devices become available.

The purpose of this document is to help designers maintain compatibility when using a member of the HCS12 D family (MC9S12Dxxx - Table 1) as an emulation tool when developing an application targeted at a member of the HCS12 B family (MC9S12Bxxx - Table 2).

Allowing for some minor constraints, as detailed in each section, code can be written for a D family device which will then run unmodified on a B family device.

This document is intended for use in conjunction with the documents listed in the **Document Reference List**. A summary of the families is provided in the **Overview of Families** followed by consideration of each peripheral module (roughly in sequence with the MC9S12DP256 Device User Guide) in the **B & D Module Summary**. Memory maps and modules containing significant differences are then covered in subsequent sections.

Overview of Families

Key points of consideration are:

- Peripheral count
  - The B family generally has a reduced peripheral set from the D family.
  - The B family does not support IIC or J1850 (BDLC).
  - B family devices have one MSCAN module and one SPI module.
- Memory maps
  - Generally a B family device of a specific Flash memory size will have less RAM and EEPROM than an equivalent D family device. Careful re-mapping of these modules is required to achieve compatible memory maps.
- Timer
  - The B family's Standard Timer is a subset of the D families Enhanced Capture Timer.
- ATD
  - The B family has a single 16 channel, 10-bit ATD as opposed to the two 8 channel, 10-bit ATDs of the D family.

A summary of feature sets of appropriate D family devices can be found in **Table 1**. A full list of all devices in the D family can be found in the D family Product Brief.

Table 1. D family Features

Flash	RAM	EEPROM	Package	Device MC9S12–	CAN	SCI	SPI	A/D	PWM**	I/O
256K	12K	4K	112LQFP	DP256	5	2	3	2/16	8	91
				DT256	3	2	3	2/16	8	91
				DG256/DJ256 *	2	2	3	2/16	8	91
			80QFP	DG256/DJ256 *	2	2	3	1/8	7	59
128K	8K	2K	112LQFP	DT128	3	2	2	2/16	8	91
				DG128/DJ128 *	2	2	2	2/16	8	91
			80QFP	DG128/DJ128 *	2	2	2	1/8	7	59
64K	4K	1K	112LQFP	D64/DJ64 *	1	2	1	2/16	8	91
			80QFP	D64/DJ64 *	1	2	1	1/8	7	59

All devices have 8 channel ECT timer & IIC modules.

* 'J' devices have J1850 (BDLC module).

**All devices have 8-channel PWM internally, only 7 channels are bonded out in 80QFP.

A summary of feature sets of the B family devices can be found in **Table 2**.

Table 2. B family Features

Flash	RAM	EEPROM	Package	Device MC9S12–	CAN	SCI	SPI	A/D	PWM**	I/O
256K	8K	2K	112LQFP	B256	1	2	1	16ch	8ch	91
			80QFP	B256	1	2	1	8ch *	7ch	59
128K	4K	1K	112LQFP	B128	1	2	1	16ch	8ch	91
			80QFP	B128	1	2	1	8ch *	7ch	59
64K	2K	1K	80QFP	B64	1	2	1	8ch *	7ch	59

All devices have an 8-channel Standard timer.

* 16 channel ATD with only 8 analog input sources bonded out.

** All devices have 8-channel PWM internally; only 7 channels are bonded out in 80QFP.

Due to the differing RAM and EEPROM sizes it is recommended that, wherever possible, development is carried out with the closest matching Flash size device, i.e. if the target is a B128 then develop with a D128, etc.

Each device will have a unique identifier value encoded in the ‘Part ID’ registers. If desired, this value may be decoded by an application and appropriate routines selected for the specific device. See **Part IDs** for details.

NOTE: *The 80-pin I/0 pitfalls, described in Engineering Bulletin EB386, are the same for both B & D families.*

B & D Module Summary

Device Memory Maps

Each device has a unique combination of memory module sizes and peripheral modules and will therefore have a different memory map. Careful re-mapping of the memory modules is required for compatibility. See **Device Memory Maps** for details. Where individual register addresses are presented in this document as $_ this indicates a module offset.

Signal Description

Packages and pin-outs are equivalent and compatible.

Where a module on a D family device is not implemented on a B family device it’s I/O functionality is not available on the appropriate ports. All other functionality of the appropriate I/O pins will be compatible.

The I/O assignment for the CAN RX & TX pins is equivalent to the default routing of CAN0 on the D family:

RXCAN pin 73/80-pin package or pin 103/112-pin package
TXCAN pin 72/80-pin package or pin 102/112-pin package

The alternative I/O routing of CAN0 is not available on the B family. See **Module Routing Register**.

System Clock

The system clock distribution is compatible.

Obviously, where modules are not implemented the clock is not routed.

Modes of Operation

Modes of Operation and security are compatible.

Resets & Interrupts/Vector tables

Resets and Interrupts are functionally compatible.

Where an interrupt is associated with a module not implemented on a B family device the vector locations will be reserved. For compatibility, these locations should remain unused and unprogrammed or, for good practice, be configured to point to a TRAP routine.

The inputs for unimplemented peripheral modules are internally tied to ground so that no interrupts for those vectors should occur.

HCS12 Core

The HCS12 Core is unchanged.

Low Power Modes, External Bus Control, Background Debug Mode and Memory Mapping are all compatible.

Clock and Reset generator (CRG)

The CRG logic is compatible.

The oscillator module on the B family will be selectable for either ‘low power Colpitts oscillator’ or ‘Pierce oscillator/external clock’ configurations, compatible with current Dx128 devices and future D family devices.

The current Dx256 devices (K79X and K36N masks) support the ‘ low power Colpitts oscillator’ or ‘external clock’ options. The pin out and oscillator circuit is compatible for either of these two options.

Timer

The B family timer (TIM) is a subset of the D family timer (ECT).

See **Timer** section for details.

Analog To Digital Converter (ATD)

The D family has two 8-channel ATD converters, the B family has a single 16-channel ATD converter. Compatibility when using eight or less channels can be achieved using ADT0 on the D family and observing a number of constraints.

Minor code changes are required to make use of analog inputs AN[15:8].

See **ATD** section for details.

Inter IC Interface (IIC)

This module is not implemented on B family.

The relevant register addresses will be reserved and should therefore not be accessed.

Serial Communications Interface (SCI)

The SCI modules are functionally compatible.

Serial Peripheral Interface (SPI)

The SPI0 module is functionally compatible.

SPI1 & SPI2 are not implemented on the target device so their relevant register addresses will be reserved and should therefore not be accessed.

Pulse Width Modulator (PWM)

The PWM module is compatible.

Flash EEPROM

Flash modules are compatible on equivalent sized devices i.e. the Flash implementation on the B256 is equivalent to the Dx256, etc.

The Flash allocation for different Flash size devices is detailed in Engineering Bulletin EB386.

EEPROM

The EEPROM modules are functionally compatible.

The EEPROM array size on comparable flash devices is generally smaller on the B family. To be ensure compatibility, usage should be limited to the array address range on the target B device and the memory mapping must be compatible (it is important to ensure that the protection/reserved field is at the same location). See **Device Memory Maps** for details.

RAM

The RAM modules are functionally compatible.

The RAM array size on comparable flash devices is generally smaller on the B family. To be ensure compatibility, usage should be limited to the array address range on the target B device and the memory mapping must be compatible. See **Device Memory Maps** for details.

MSCAN

The MSCAN0 module is functionally compatible.

MSCAN 1,2,3 & 4 are not implemented on the B family and their registers addresses will be reserved and should therefore not be accessed.

Alternative routing of CAN0 I/O is not available on the B family.

Port Integration Module (PIM)

Since the parts each have a different set of peripherals, some minor differences in the PIM must be considered. The PIM modules on all B & D family devices contain the same Port control & status registers and are compatible when used for general purpose I/O.

As each device has a different number of peripherals requiring I/O multiplexing, some of the functionality of the larger devices will not be available on a smaller device where an equivalent module isn't implemented. As this multiplexing occurs automatically as peripherals are enabled or disabled there are no compatibility issues.

Where a module on a D family device is not implemented on a B family device it's functionality is not available on the appropriate I/O pins. For example the MSCAN3 & MSCAN4 modules are only available on the MC9S12DP256 therefore on B devices Port M pins PTM6 and PTM7 will be general purpose I/O only.

Module Routing Register

	Bit 7	6	5	4	3	2	1	Bit 0
				MODRR4				
Reset:	0	0	0	0	0	0	0	0

Figure 1. Module Routing Register (MODRR)

Read: anytime.
Write: anytime.

On the B family, I/O re-routing is available for the SPI0 module.

Bit MODRR[4] selects between Port S[7:4] pins (the default; only available in the 112-pin package) and Port M[5:2] pins. See **Table 3**.

Table 3. MODRR[4] — SPI0 Routing

MODRR[4]	MISO0	MOSI0	SCK0	SS0
0	PS4	PS5	PS6	PS7
1	PM2	PM4	PM5	PM3

NOTE: *On the D family, CAN0 I/O can be re-routed to allow the BDLC module to control Port M pins PM0 and PM1. As there is no BDLC module on the B family, there is no MODRR support for alternative routing*

Where a peripheral is not implemented, its associated MODRR control bits can be written with no effect and will read back as zero.

Voltage Regulator (VREG)

The VREG is compatible.

Power supply layout for the D family devices will be compatible for B family targets.

BDLC

This module (on the DJ devices) is not implemented on B family. The relevant register addresses will be reserved and should therefore not be accessed.

Part IDs

The part ID on each device is “coded” in two 8-bit registers, PARTIDH and PARTIDL (address offset $_1A and $_1B), in the Core register block. The read-only value is a unique part ID for each revision of any device.

Bits 7:4 of PARTIDH contain the family identifier.
Bits 3:0 of PARTIDH contain the family member identifier.

The PARTIDH values for D family devices is shown in **Table 4**.

Table 4. D family Device ID Value

D family Device	PARTIDH
MC9S12Dx256	$00
MC9S12Dx128	$01
MC9S12Dx64	$02
MC9S12Dx32	$03

The PARTIDH values for B family devices is shown in **Table 5**.

Table 5. B family Device ID Value

B family Device	PARTIDH
MC9S12B256	$20
MC9S12B128	$21
MC9S12B64	$22

The PARTIDL value will be unique for each silicon revision.

Device Memory Maps

Peripheral Module Map

A comparison of the Register Block memory maps of the 9S12DP256 and the B family devices following reset is provided in **Table 6**.

Table 6. Register Block Memory Map Comparison

Address on Reset	MC9S12DP256 Module	B Family Module	Size (Bytes)
$0000 – $0017	CORE (Ports A, B, E, Modes, Inits, Test)	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 – $0019	Reserved	Reserved	2
$001A – $001B	CORE (Device ID register (PARTID))	CORE (Device ID register (PARTID))	2
$001C – $001F	CORE (MEMSIZ, IRQ, HPRIO)	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 – $0027	Reserved	Reserved	8
$0028 – $002F	CORE (Background Debug Mode)	CORE (Background Debug Mode)	8
$0030 – $0033	CORE (PPAGE, Port K)	CORE (PPAGE, Port K)	4
$0034 – $003F	Clock and Reset Generator (PLL, RTI, COP)	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 – $006F	Enhanced Capture Timer 16-bit 8 channels	Standard Timer 16-bit 8 channels	48
$0070 – $007F		**Reserved**	16
$0080 – $009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	Analog to Digital Converter 10-bit **first 8 channels** (ATD) *	32
$00A0 – $00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	Pulse Width Modulator 8-bit 8 channels (PWM)	40
$00C8 – $00CF	Serial Communications Interface 0 (SCI0)	Serial Communications Interface 0 (SCI0)	8

Table 6. Register Block Memory Map Comparison

Address on Reset	MC9S12DP256 Module	B Family Module	Size (Bytes)
$00D0–$00D7	Serial Communications Interface 1 (SCI1)	Serial Communications Interface 1 (SCI1)	8
$00D8–$00DF	Serial Peripheral Interface (SPI0)	Serial Peripheral Interface (SPI0)	8
$00E0–$00E7	**Inter IC Bus**	**Reserved**	8
$00E8–$00EF	**Byte Data Link Controller (BDLC)**	**Reserved**	8
$00F0–$00F7	Serial Peripheral Interface (SPI1)	Serial Peripheral Interface (SPI1)	8
$00F8–$00FF	**Serial Peripheral Interface (SPI2)**	**Reserved**	8
$0100–$010F	Flash Control Register	Flash Control Register	16
$0110–$011B	EEPROM Control Register	EEPROM Control Register	12
$011 –$011F	Reserved	Reserved	4
$0120–$012B	**Analog to Digital Converter 10-bit 8 channels (ATD1)**	**Reserved**	13
$012D		ATDDIEN0 *	1
$012E		**Reserved**	1
$012F		PORTAD0 *	1
$012F–$013F		**Reserved**	16
$0140–$017F	Motorola Scalable Can (CAN0)	Motorola Scalable Can (CAN0)	64
$0180–$01BF	**Motorola Scalable Can (CAN1)**	**Reserved**	64
$01C0–$01FF	**Motorola Scalable Can (CAN2)**	**Reserved**	64
$0200–$022F	**Motorola Scalable Can (CAN3)**	**Analog to Digital Converter 10-bit 16 channels (ATD)**	48
$0230–$023F		**Reserved**	16
$0240–$027F	Port Integration Module (PIM)	Port Integration Module (PIM)	64
$0280–$02BF	**Motorola Scalable Can (CAN4)**	**Reserved**	64
$02C0–$03FF	Reserved	Reserved	320

Bold indicates differences

* These registers are also accessible in the ATD register space. See **FIFO mode**.

The Register block can be re-mapped to any 2K boundary in the 64K memory map.

For compatibility, the registers in the reserved sections on the B family target device should not be accessed when developing an application with a D family device.

Register block, RAM & EEPROM Maps

Device maps

The following tables compare the device maps of similarly sized Flash devices from the D & B families following reset.

Table 7. 256K Flash Memory Map Following Reset

	Dx256	B256
Registers	$0000–$03FF: 1K	$0000–$03FF: 1K
RAM	$1000–$3FFF: 12K	$0000–$1FFF: 8K ($0000–$03FF: 1K not visible)
EEPROM	$0000–$0FFF: 4K ($0000–$03FF: 1K not visible)	$0000–$07FF: 2K (not visible)

Table 8. 128K Flash Memory Map Following Reset

	Dx128	B128
Registers	$0000–$03FF: 1K	$0000–$03FF: 1K
RAM	$0000–$1FFF: 8K ($0000–$03FF not visible)	$0000–$0FFF: 4K ($0000–$03FF: 1K not visible)
EEPROM	$0000–$07FF: 2K (not visible)	$0000–$07FF: 1K (not visible) *

* A 1K EEPROM module appears in a 2K space twice, at $0000–$03FF and $0400–$07FF. The protection/reserved field also appears twice at $03F0–$03FF and $07F0–$07FF.

Table 9. 64K Flash Memory Map Following Reset

	Dx64	B64
Registers	$0000–$03FF: 1K	$0000–$03FF: 1K
RAM	$0000–$0FFF: 4K ($0000–$03FF: 1K not visible)	$0800–$0FFF: 2K
EEPROM	$0000–$03FF: 1K (not visible) *	$0000–$07FF: 1K (not visible) *

* A 1K EEPROM module appears in a 2K space twice, at $0000–$03FF and $0400–$07FF. The protection/reserved field also appears twice at $03F0–$03FF and $07F0–$07FF.

Re-mapping

When using a D family device to emulate a B family device, a compatible memory map must be used to ensure that the equivalent memory is accessed at the same locations on each device.

Three ‘Position Registers’ in the Core register block control the location of the memory blocks:

- INITRG – Initialization of Internal Registers Position Register
- INITRM – Initialization of Internal RAM Position Register
- INITEE – Initialization of Internal EEPROM Position Register

To ensure compatibility the D device map must be a superset of the target B device map. For software compatibility the maps should be valid for the same Position Register values and the top of the EEPROM maps should be aligned so that the protection/ reserved field is at the same address.

The rules that control the re-mapping of memory blocks are well documented in Engineering Bulletin EB386 and the recommended options for the Position Registers are also valid for the B family. **Table 10** and **Table 11** show examples of compatible mappings.

```
INITRG = 0x00;
INITRM = 0x39;
INITEE = 0x09;
```

Table 10. Re-mapping to locate the registers block in the direct page

Device	Registers	RAM	EEPROM
B256	$0000–$03FF	$2000–$3FFF	$0800–$0FFF
B128	$0000–$03FF	$3000–$3FFF	$0800–$0FFF *
B64	$0000–$03FF	$3800–$3FFF	$0800–$0FFF *

* The1K EEPROM module appears twice, at $0800–$0BFF and $0C00–$0FFF. For compatibility, access the EEPROM in the range $0C00–$0FFF. This locates the protection/reserved field at $0FF0–$0FFF on all devices.

```
INITRG = 0x30;
INITRM = 0x00;
INITEE = 0x39;
```

Table 11. Re-mapping to locate the RAM in the direct page

Device	Registers	RAM	EEPROM
B256	$3000–$33FF	$0000–$1FFF	$3800–$3FFF
B128	$3000–$33FF	$0000–$0FFF	$3800–$3FFF
B64	$3000–$33FF	$0000–$07FF	$3800–$3FFF

* The1K EEPROM module appears twice, at $3800–$3BFF and $3C00–$3FFF. For compatibility, access the EEPROM in the range $3C00–$3FFF. This locates the protection/reserved field at $3FF0–$3FFF on all devices.

Using the above options ensures that any D family device of an equivalent or larger Flash size will have a compatible memory map.

Using D256 & D128 devices to emulate the B64 restricts access to the non-paged Flash at $0000-$3FFF as there is no flash at this location on these devices.

When using a D64 to emulate a B64 device the flash is equivalent but the RAM is larger on the D64 and will restrict access to 2K of the non-paged Flash with the above mappings.

These are not the only possible configurations and alternative mappings may be more effective for some applications. For example where one of the modules might be mapped over the Flash to allow a window to external memory or where modules might be mapped over the paged window ($8000-$BFFF) to maximize access to the non-paged memory.

Timer

The B family has a Standard Timer (TIM_16B8C) with

- A 16-bit free running timer
- A timer overflow to extend the 16-bit range of the counter
- Up to eight output compare functions (O/C).
- Up to eight input capture functions (I/C).
- A 16-bit Pulse Accumulator on channel-7 (Gated Time Accumulation and Event Counter modes).

The D family has an Enhanced Capture Timer (ECT_16B8C) which is a superset of the Standard timer. The following features are not available on the B family timer:

- 16-bit buffer registers on input capture channels 0 to 3.
- User selectable Delay counters on channels 0 to 3 for increased noise immunity.
- A 2nd 16-bit Pulse Accumulator (Event Counter Mode) on channel 0.
- Four 8-bit, buffered Pulse Accumulators (Event Counter Mode) on channels 0 to 3 (these share registers with the two 16-bit PA so you can have either one 16-bit PA or two 8-bit PA in each case).
- A 16-bit Modulus Down Counter with 4-bit prescaler. Controls the transfer period of data into the I/C or PA buffers in Latch Modes and/or generates a periodic interrupt.

NOTE: *On the ECT, the Standard Timer 16-bit PA is called Pulse Accumulator A.*

Timer Registers

Timer Memory Maps

B family memory map (TIM)

$0040 to $006F following reset (48 bytes)

D family memory map (ECT)

$0040 to $007F following reset (64 bytes)

On the B family, the registers from module offset $_30 to $_3F are reserved and should not be written.

All of the enhanced features default to disabled following reset so a simple rule for compatibility is don't access any registers above module offset $_23 on the ECT as these are reserved on the B family.

The register map for the B family timer is shown in **Table 12**.

Table 12. B family Standard Timer Register Summary

Module Offset	Use	Name
$_00	Timer Input Capture/Output Compare Select	TIOS
$_01	Timer Compare Force Register	CFORC
$_02	Output Compare 7 Mask Register	OC7M
$_03	Output Compare 7 Data Register	OC7D
$_04	Timer Count Register High	TCNT
$_05	Timer Count Register Low	TCNT
$_06	Timer System Control Register1	TSCR1
$_07	Timer Toggle Overflow Register	TTOV
$_08	Timer Control Register1	TCTL1
$_09	Timer Control Register2	TCTL2
$_0A	Timer Control Register3	TCTL3
$_0B	Timer Control Register4	TCTL4
$_0C	Timer Interrupt Enable Register	TIE
$_0D	Timer System Control Register2	TSCR2
$_0E	Main Timer Interrupt Flag1	TFLG1
$_0F	Main Timer Interrupt Flag2	TFLG2
$_10	Timer Input Capture/Output Compare Register0 High	TC0
$_11	Timer Input Capture/Output Compare Register0 Low	TC0
$_12	Timer Input Capture/Output Compare Register1 High	TC1

Table 12. B family Standard Timer Register Summary

Module Offset	Use	Name
$_13	Timer Input Capture/Output Compare Register1 Low	TC1
$_14	Timer Input Capture/Output Compare Register2 High	TC2
$_15	Timer Input Capture/Output Compare Register2 Low	TC2
$_16	Timer Input Capture/Output Compare Register3 High	TC3
$_17	Timer Input Capture/Output Compare Register3 Low	TC3
$_18	Timer Input Capture/Output Compare Register4 High	TC4
$_19	Timer Input Capture/Output Compare Register4 Low	TC4
$_1A	Timer Input Capture/Output Compare Register5 High	TC5
$_1B	Timer Input Capture/Output Compare Register5 Low	TC5
$_1C	Timer Input Capture/Output Compare Register6 High	TC6
$_1D	Timer Input Capture/Output Compare Register6 Low	TC6
$_1E	Timer Input Capture/Output Compare Register7 High	TC7
$_1F	Timer Input Capture/Output Compare Register7 Low	TC7
$_20	16-Bit Pulse Accumulator A Control Register	PACTL
$_21	Pulse Accumulator A Flag Register	PAFLG
$_22	Pulse Accumulator Count Register(3) High	PACNT (PACN3)
$_23	Pulse Accumulator Count Register(2) Low	PACNT (PACN2)
$_24 – $_2B	* Reserved –	
$_2C	* Reserved –	
$_2D	Timer Test Register	TIMTST
$_2E	* Reserved –	
$_2F	* Reserved –	

* Write has no effect, Read returns $00.

Timer Interrupts

The following vectors are common to the D & B family timers:

```
$FFEE-$FFEF      Timer channel 0
$FFEC-$FFED      Timer channel 1
$FFEA-$FFEB      Timer channel 2
$FFE8-$FFE9      Timer channel 3
$FFE6-$FFE7      Timer channel 4
$FFE4-$FFE5      Timer channel 5
$FFE2-$FFE3      Timer channel 6
$FFE0-$FFE1      Timer channel 7
$FFDE-$FFDF      Timer overflow
$FFDC-$FFDD      Pulse accumulator (A) overflow
$FFDA-$FFDB      Pulse accumulator (A) input edge
```

On the D family, these additional interrupts support the enhanced features of the ECT:

```
$FFCA-$FFCB      Modulus Down Counter Underflow
$FFC8-$FFC9      Pulse Accumulator B Overflow
```

On the B family these two vector locations are reserved. For compatibility, they should remain unused and unprogrammed or, for good practice, be configured to point to a TRAP routine.

ATD

The HCS12 ATD converter is based on a modular design. The D family ATD module (referred to as D_ATD) and B family ATD module (referred to as B_ATD) are variants of the core HCS12 ATD optimised for the two different families. The actual analog conversion module and I/O is of the same design. Generally the control and functionality of the two modules is very similar.

Each ATD converter can be configured for clock speed, sample time period, conversion resolution, result data format and interaction with MCU modes.

Conversion sequences define which analog source to start conversion at and (if multiple conversions are selected) how many sequential conversions to carry out. Scan mode can be selected to continuously repeat a conversion sequence.

A conversion sequence is initiated by a write to the ATDCTL5 register and, if enabled, a valid signal on an external trigger input.

Definitions used in this document:

- PADxx – port pin used for general purpose digital input.
- ANxx – Analog signal input pin.
- ADxx – analog converter input channel.

The D family has two independent 8 channel, 10-bit ATD modules (ATD_10B8C) each with:

- Analog Input Multiplexer for 8 Analog Input Channels.
- 1 to 8 Conversion Sequence Lengths.
- External trigger on channel AN07 (ATD0) & AN15 (ATD1).
- i/p channel wrap around at AD07.

The B family has a single 16 channel, 10-bit ATD (ATD_10B16C) module (which is in many aspects a superset of the D_ATD module) with:

- Analog Input Multiplexer for 16 Analog Input Channels.
- 1 to 16 Conversion Sequence Lengths.
- External trigger on channel AN15.
- i/p channel wrap around at AD15.

Compatibility Constraints

Applications requiring greater than 8 analog inputs will require code changes. Compatibility for greater than 8 channels is not considered in this document.

Where an application's requirements can be met with a single 8-channel D_ATD (ATD0) it is possible to achieve compatibility allowing for certain constraints:

- Input channel wrap-around is not compatible (**Input Channel Wrap Around**).
- FIFO mode is not compatible (**FIFO mode**).
- External trigger is not available (**External Trigger Source**).

With careful planning of conversion sequences the flexibility of conversions available on the D_ATD can be maintained (**Design Analysis**).

Design Analysis

Doing an analysis of the ATD sources to be converted can maximize compatibility.

Key information on each analog source should be evaluated:

- Period of conversion (how often is the conversion required?)
- Is continuous scanning required?
- Source impedance – this can affect the required sample time or ATD clock frequency?
- Required resolution?
- Critical conversion time?

Sources with similar requirements can then be grouped onto adjacent ATD inputs and the ATD configured appropriately for each conversion sequence.

If there is a multiple channel selection that requires continuous scanning (SCAN bit = 1) it should be grouped starting at AN0 (**Input Channel Wrap Around**).

Input Channel Wrap Around

On the D_ATD, in the case of a multiple conversion sequence (MULT bit = 1), when the input selector goes past AD7 it wraps to AD0.
On the D family, ATD input AD7 of ATD0 is connected to pin AN07.

On the B_ATD, in the case of a multiple conversion sequence (MULT bit = 1), when the input selector goes past AD15 it wraps to AD0.
On the B family, ATD input AD15 is connected to pin AN15. The input selector does not wrap following conversion of AN07.

For compatibility do not use conversion sequences that go past ATD input AD7.

Example: if a 4 channel conversion sequence is executed starting with AD6 the results registers will contain results as shown in **Table 13**.

Table 13. ATD results for Example1

Result	ATD0 (D_ATD)	B_ATD
ATDDR0/ATD**0**DR0	AD6	AD6
ATDDR1/ATD**0**DR1	AD7	AD7
ATDDR2/ATD**0**DR2	AD0	AD8
ATDDR3/ATD**0**DR3	AD1	AD9
ATDDR4/ATD**0**DR4	AD2	AD10

Compatible continuous scanning of the above conversion sequence is not possible.

In order to avoid this difference in behaviour either

a. Split the above conversion sequence into two sequences so that the conversion does not cross the AD7/AD0 boundary, i.e. use a 2 channel conversion starting at AD6 followed by a 3 channel conversion starting at AD0. The results might be moved to a separate array by software.
b. Group channels at the design stage so that any multiple conversion sequences do not cross the AD7/AD0 boundary, i.e. allocate the 5 signals to AN[0:4] and use a 5 channel conversion starting at AD0. This is compatible for continuous scanning (see **Design Analysis**).

FIFO mode

FIFO mode is incompatible due to the increase in FIFO depth – 2x8 deep FIFOs on the D family and 1x 16 deep FIFO on the B family.

For compatibility FIFO mode should not be used.

External Trigger Source

On the D family each ATD converter has an external trigger source located on channel AD07.

On ATD0 the external trigger source is on i/p AN07.

On the B family there is only one external trigger source on channel AD15/input AN15.

For compatibility the external trigger feature should not be used.

ATD Interrupts

This vector is common to the B and D family ATD:

```
$FFD2-$FFD3    ATD/ATD0
```

On the D family, this additional interrupt supports the 2nd ATD module:

```
$FFD0-$FFD1    ATD1
```

On the B family this vector location is reserved. For compatibility, it should remain unused and unprogrammed or, for good practice, be configured to point to a TRAP routine.

ATD Memory Maps

D family memory map following reset (2 x ATD_10B8C)

```
$0080-$009F      ATD0     (32 bytes)
$0120-$013F      ATD1     (32 bytes)
```

B family memory map following reset (1 x ATD_10B16C)

```
$0200-$023F      ATD      (48 bytes)
```

NOTE: *On the D family this location contains the CAN3 module*

On the B family, ATD registers $_00 to $_1F are also accessible at $0080 to $009F following reset i.e. they can be accessed at either location (indicated by ** in **Table 14**). This is to support software compatibility with the D family ATD0.

On the B family, register ATDDIEN0 can also be accessed at $012D and register PORTAD0 can also be accessed at $012F, following reset. This is to support software compatibility with the D family where digital inputs PAD08 to PAD15 are used.

The remaining locations of the ATD1 module registers on the D family are reserved and should not be written on the B family.

The register map for the B family ATD is shown in **Table 14**.

Table 14. B family ATD Register Summary

Address Offset	Use	Name	Access
$_00	ATD Control Register 0	ATDCTL0 **	*
$_01	ATD Control Register 1	ATDCTL1**	*
$_02	ATD Control Register 2	ATDCTL2 **	R/W
$_03	ATD Control Register 3	ATDCTL3 **	R/W
$_04	ATD Control Register 4	ATDCTL4 **	R/W
$_05	ATD Control Register5	ATDCTL5 **	R/W
$_06	ATD Status Register 0	ATDSTAT0 **	R/W

Table 14. B family ATD Register Summary

Address Offset	Use	Name	Access
$_07	Reserved	**	–
$_08	ATD Test Register 0	ATDTEST0 **	*
$_09	ATD Test Register 1	ATDTEST1 **	*
$_0A	**ATD Status Register 2**	**ATDSTAT2 ****	**R/W**
$_0B	ATD Status Register 1	ATDSTAT1 **	R/W
$_0C	**ATD Input Enable Register 0**	**ATDDIEN0 ****	**R/W**
$_0D	ATD Input Enable Register	ATDDIEN1 **	R/W
$_0E	**ATD Port Data Register 0**	**PORTAD0 ****	**R**
$_0F	ATD Port Data Register 1	PORTAD1 **	R
$_10, $_11	ATD Result Register	ATDDR0H, ATDDR0L **	R/W
$_12, $_13	ATD Result Register 1	ATDDR1H, ATDDR1L **	R/W
$_14, $_15	ATD Result Register 2	ATDDR2H, ATDDR2L **	R/W
$_16, $_17	ATD Result Register 3	ATDDR3H, ATDDR3L **	R/W
$_18, $_19	ATD Result Register 4	ATDDR4H, ATDDR4L **	R/W
$_1A, $_1B	ATD Result Register 5	ATDDR5H, ATDDR5L **	R/W
$_1C, $_1D	ATD Result Register 6	ATDDR6H, ATDDR6L **	R/W
$_1E, $_1F	ATD Result Register 7	ATDDR7H, ATDDR7L **	R/W
$_20, $_21	**ATD Result Register 8**	**ATDDR8H, ATDDR8L**	**R/W**
$_22, $_23	**ATD Result Register 9**	**ATDDR9H, ATDDR9L**	**R/W**
$_24, $_25	**ATD Result Register 10**	**ATDDR10H, ATDDR10L**	**R/W**
$_26, $_27	**ATD Result Register 11**	**ATDDR11H, ATDDR11L**	**R/W**
$_28, $_29	**ATD Result Register 12**	**ATDDR12H, ATDDR2L**	**R/W**
$_2A, $_2B	**ATD Result Register 13**	**ATDDR13H, ATDDR13L**	**R/W**
$_2C, $_2D	**ATD Result Register 14**	**ATDDR14H, ATDDR14L**	**R/W**
$_2E, $_2F	**ATD Result Register 15**	**ATDDR15H, ATDDR15L**	**R/W**

Bold indicates the additional registers of the 16-channel B_ATD

*Factory test only.

** Aliased into ATD0 space.

Additional Registers on the B_ATD

ATD Status Register 2 (ATDSTAT2)

Read-only register containing the Conversion Complete Flags CCF15 to CCF8, for the upper 8 channels.

There is no equivalent register on the D family.

BIT	7	6	5	4	3	2	1	0
R	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2. ATD Status Register 2 (ATDSTAT2)

Read: anytime
Write: No Effect.

CCFx — Conversion Complete Flag x (x= 15, 14, 13, 12, 11, 10, 9, 8)

A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags are associated with the conversion position in a sequence (and also the result register number).

Therefore, CCF8 is set when the ninth conversion in a sequence is complete and the result is available in result register ATDDR8; CCF9 is set when the tenth conversion in a sequence is complete and the result is available in ATDDR9, and so forth. A flag CCFx (x= 15, 14, 13, 12, 11, 10, 9, 8) is cleared when one of the following occurs:

a. Write to ATDCTL5 (a new conversion sequence is started)
b. If AFFC=0 and read of ATDSTAT2 followed by read of result register ATDDRx
c. If AFFC=1 and read of result register ATDDRx

1 = Conversion number x has completed, result ready in ATDDRx
0 = Conversion number x not completed

ATD Input Enable Register 0 (ATDDIEN0)

Register containing the Digital Input Enable bits for pins AN8 to AN15.

On a D family device this functionality is provided by the equivalent ATDDIEN register of ATD1.

BIT	7	6	5	4	3	2	1	0
R W	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3. Input Enable Register 0 (ATDDIEN0)

Read: anytime
Write: anytime

IENx — ATD Digital Input Enable on channel x (x= 15, 14, 13, 12, 11, 10, 9, 8)

This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register.

1 = Enable digital input buffer to PTADx.
0 = Disable digital input buffer to PTADx

NOTE: *Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.*

ATD Port Data Register 0 (PORTAD0)

Read-only register containing the digital input value for the upper 8 ATD inputs.

The data port associated with the ATD is input-only. The port pins are shared with the analog A/D inputs AN15-8.

On a D family device this functionality is provided by the equivalent PORTAD register of ATD1

.

BIT	7	6	5	4	3	2	1	0
R	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
W								
RESET:	1	1	1	1	1	1	1	1
Pin Func-tion	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8

= Unimplemented or Reserved

Figure 4. Port Data Register 0 (PORTAD0)

Read: anytime
Write: anytime, writes to this register have no effect

The A/D input channels may be used for general purpose digital input.

PTADx — A/D Channel x (ANx) Digital Input (x= 15, 14, 13, 12, 11, 10, 9, 8)

If the digital input buffer on the ANx pin is enabled (IENx=1) read returns the logic level on ANx pin (signal potentials not meeting VIL or VIH specifications will have an indeterminate value)).

If the digital input buffers are disabled (IENx=0), read returns a “1”.

Reset sets all PORTAD0 bits to “1”.

ATD Conversion Result Registers (ATDDR8 – ATDDR15)

These results registers are used to store the results of conversions 8 to 15 in a conversion sequence. They have the same format as results registers ATDDR0 – ATDDR7 (as on the D family ATD).

Registers on the B_ATD containing additional bits

ATDCTL3 – Conversion Sequence Length

On the D_ATD the max conversion sequence length is 8.

On the B_ATD it is 16.

BIT	7	6	5	4	3	2	1	0
R	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
W								
RESET:	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 5. ATD Control Register 3 (ATDCTL3)

For 8 channel compatibility with ATD0 do not use all zeros to specify the maximum sequence length and use ‘x1000xxx’ when selecting conversions on the D family.

Only select conversion lengths of eight or less and ensure that for multiple conversion sequences the sequence length does not result in a conversion of i/p AN08 (See **FIFO mode**).

D family ATD Conversion Sequence coding is shown in **Table 15** and **Table 16**.

Table 15. D family Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions Per Sequence
0	0	0	0	8
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	8

X = don’t care

Table 16. B family Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions Per Sequence
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

ATDCTL5 – Analog Input Channel Selection

	7	6	5	4	3	2	1	0
R W	DJM	DSGN	SCAN	MULT	**0**	CC	CB	CA
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6. D family ATD Control Register 5 (ATDCTL5)

BIT	7	6	5	4	3	2	1	0
R W	DJM	DSGN	SCAN	MULT	**CD**	CC	CB	CA
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7. B family ATD Control Register 5 (ATDCTL5)

On the D family each converter selects from 8 Analog sources.

On the B family converter selects from 16 Analog sources.

For 8-channel compatibility on the B family always write CD to zero.

Note that for multiple channel conversion sequences the CD/CC/CB/CA bits select the first channel of the sequence.

D family Analog Input Channel Selection coding is shown in **Table 17** and **Table 18**.

Table 17. ATD0 Analog Input Channel Selection coding

CC	CB	CA	Analog Input Channel
0	0	0	AD0
0	0	1	AD1
0	1	0	AD2
0	1	1	AD3
1	0	0	AD4
1	0	1	AD5
1	1	0	AD6
1	1	1	AD7

Table 18. ATD1 Analog Input Channel Selection coding

CC	CB	CA	Analog Input Channel
0	0	0	AD8
0	0	1	AD9
0	1	0	AD10
0	1	1	AD11
1	0	0	AD12
1	0	1	AD13
1	1	0	AD14
1	1	1	AD15

Table 19. B family Analog Input Channel Selection coding

CD	CC	CB	CA	Analog Input Channel
0	0	0	0	AD0
0	0	0	1	AD1
0	0	1	0	AD2
0	0	1	1	AD3
0	1	0	0	AD4
0	1	0	1	AD5
0	1	1	0	AD6
0	1	1	1	AD7
1	0	0	0	AD8
1	0	0	1	AD9
1	0	1	0	AD10
1	0	1	1	AD11
1	1	0	0	AD12
1	1	0	1	AD13
1	1	1	0	AD14
1	1	1	1	AD15

ATDSTAT0 – Conversion Complete Flags

	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	**0**	CC2	CC1	CC0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8. D family ATD Status Register 0 (ATDSTAT0)

BIT	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	**CC3**	CC2	CC1	CC0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9. B family ATD Status Register 0 (ATDSTAT0)

On the D family each converter has a three bit conversion counter to track up to 8 channel conversion sequences.

On the B family converter there is a 4 bit conversion counter to track up to 16 channel conversion sequences.

For conversion sequences of 8-channels or less CCR will always read ‘0’.

Document Reference List

Additional information can be found in:

The MC9S12D family PRODUCT Brief (MC9S12D-familyPP).

The MC9S12B family PRODUCT Proposal (MC9S12B-FamilyPP).

Engineering Bulletin EB377 “Change Summary of the MC9S12DP256 mask set 0K79X versus 0K36N”. (doc EB377/D). *

Engineering Bulletin EB386 “HCS12 D-family Compatibility Considerations”. (doc EB386/D). *

The 9S12DP256 User Guides for K79X mask sets (ZIP format) 9S12DP256 – ZIP *. Includes:

MC9S12DP256 Device User Guide	(9S12DP256UG/D)
PIM_9DP256 Block User Guide	(9S12DP256PIMUG/D)
FTS256K Block User Guide	(S12FTS256KUG/D)
EETS4K Block User Guide	(S12EETS4KUG/D)
HCS12 V1.5 Core User Guide	(S12CPU15UG/D)
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ECT_16B8C Block User Guide	(S12ECT16B8CUG/D)
ATD_10B16C Block User Guide	(S12ATD10B16CUG/D)
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SPI Block User Guide	(S12SPIUG/D)
PWM_8B8C Block User Guide	(S12PWM8B8CUG/D)
MSCAN Block User Guide	(S12MSCANUG/D)
VREG Block User Guide	(S12VREGUG/D)

The 9S12DTB128 User Guide (ZIP format) 9S12DP256 – ZIP *. Also Includes:

MC9S12DT128 Device User Guide	(9S12DT128UG/D)
PIM_9DTB128 Block User Guide	(9S12DTB128PIMUG/D)
FTS128K Block User Guide	(S12FTS128KUG/D)
EETS2K Block User Guide	(S12EETS2KUG/D)

HC9S12 16-bit 8-channel TIM Block User Guide (S12TIM16B8CUG/D).*

HC9S12 10-bit 16-channel ATD Block User Guide (S12ATD10B16CUG/D).*

* At the time of publication all of these documents were available on line at:

http://www.motorola.com/semiconductors

All appropriate device Mask Set Errata should also be referenced.

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